MODELING, DESIGN AND DEMONSTRATION OF ULTRA-SHORT, FINE-PITCH SOLDER-BASED INTERCONNECTION SYSTEMS WITH HIGH-THROUGHPUT ASSEMBLY

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Ting-Chia (Nathan) Huang

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MODELING, DESIGN AND DEMONSTRATION OF ULTRA-SHORT, FINE-PITCH SOLDER-BASED INTERCONNECTION SYSTEMS WITH HIGH-THROUGHPUT ASSEMBLY

Approved by:

Dr. Rao R. Tummala, Advisor
School of Materials Science and Engineering
Georgia Institute of Technology

Dr. Suresh Sitaraman
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Naresh Thadhani
School of Materials Science and Engineering
Georgia Institute of Technology

Dr. Raj Pulugurtha
School of Materials Science and Engineering
Georgia Institute of Technology

Dr. Eric Vogel
School of Materials Science and Engineering
Georgia Institute of Technology

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Dedicated to my parents, Hank and Joyce

And to my wife, Jennifer

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LIST OF ABBREVIATION

Abbreviation	Explanation
AC	Alternating current
AFM	Atomic force microscope
BEI	Backscattered electron image
BGA	Ball grid array
BSE	Backscattered electron
BMVs	Blind micro-vias
BNUF	B-stageable nonflow underfill
C4	Controlled collapse chip connection
CTE	Coefficient of thermal expansion
C-SAM	C-Mode Scanning Acoustic Microscopy
CSP	Chip scale package
D/B	Die bonding
DBC	Direct bond copper
DC	Direct current
DIP / DIL	Dual in line package
DOE	Design of experimental
EM	Electromigation
FC	Flip chip
FEM / FEA	Finite element method / Finite element analysis
FIB	Focus ion beam
FT-IR	Fourier transform infrared spectroscopy

IMC	Intermetallic
PECVD	Plasma-enhanced chemical vapor deposition
PGA	Pin grid array
SEM	Scanning electron microscope
SLID bonding	Solid-liquid interdiffusion bonding
SMT	Surface mount technology
SoC	System on chip
SoP	System on package
TC-bonding / TCB	Thermocompression bonding
TCT	Thermal cycling test
TIM	Thermal interface material
TLP	Transient liquid phase
TM	Thermomigration
TSVs	Through silicon vias
TPVs	Through package vias
NCP	Nonconductive paste
NCF	Nonconductive film
OSATs	Outsourced semiconductor assembly and test providers
WLUF	Wafer-level underfill
XEDS	X-ray Energy-dispersive spectroscopy
XPS	X-ray photoelectron microscopy
XRF	X-ray fluorescence

SUMMARY

Emerging high-performance computing systems have been driving the need for advanced packaging solutions such as high-density 2.5D interposer packages with escalating pitch, performance, and reliability requirements for off-chip interconnections. The objectives of this research are to design, develop and demonstrate novel, manufacturable, solder-based interconnection and assembly technologies at 20µm pitch, addressing the scalability limitations of conventional Cu pillars in terms of thermomechanical reliability, thermal stability and power-handling capability.

Pitch scaling with solders is accompanied by a necessary reduction in solder volume and subsequent increase in the volumetric contribution of intermetallics, raising serious concerns for stress management and reliability. Fine control of interfacial reactions is, therefore, key in extending solder-based interconnections to finer pitches and constitutes the first challenge addressed in this thesis. Intermetallic formation is primarily governed by the assembly process and the surface metallurgy that reacts with the solder, with the specific challenges and associated research tasks defined below.

From assembly perspective, pitch scaling brings a shift from conventional reflow to thermocompression bonding. Leading-edge TC-NCP (thermocompression with non-conductive paste) processes, first established by Amkor, have shown high promises for fine-pitch assembly at 40µm pitch and below. Through dynamic control of the temperature gradient in the assembled package, TC-NCP enables shorter reaction times and improved solder collapse and assembly yield. However, thermocompression processes inherently have to be customized for any given package design, with no existing guidelines for process

design. A fundamental understanding of TC-NCP is, therefore, required to design thermal and force profiles that provide accurate control over the reaction. This is the objective of the first research task. Finite element modeling of the heat transfer in TC assembly considering tool – materials – package interactions was first established and validated experimentally to provide guidelines for optimization of assembly profiles. The developed methodology was applied to design the bonding profiles used to build all specimens in this thesis. This research also enabled the first demonstration of thermocompression assembly on high-density, ultra-thin glass substrates.

Intermetallic growth in solder interconnection systems has also been traditionally controlled through the reacting surface metallurgy applied on the substrate pads. Over the last decade, standard ENEPIG (electroless Ni – electroless Pd – immersion Au) finish has been the metallurgy of choice in high-end applications for its outstanding reliability. However, the typically high thicknesses of Ni in ENEPIG limits its pitch scalability and degrades its high-frequency performance. Novel, Ni-free, metallic surface finishes are, therefore, required to meet the needs of emerging high-performance systems and form reliable interconnections at 20µm pitch with less than 10µm solder height. With such limited solder volume, risks of Au embrittlement and subsequent joints failure are also increased. The second research task addresses these challenges with the design of a new metallurgical system for reliable, ultra-short Cu pillar interconnections, based on the novel electroless Pd autocatalytic Au (EPAG) finish supplied by Atotech GmbH. The EPAG composition was optimized based on a comprehensive study including wettability testing, analysis of interfacial reactions, shear testing and thermal cycling. The optimal finish composition yielded a unique reaction with formation of a single intermetallic, resistant to

Au embrittlement. Cu pillar assemblies with the optimized EPAG composition exhibited a 3x improvement in fatigue life compared to assemblies with standard ENEPIG with less than 10µm solder height, demonstrating potential scalability of the Cu pillar technology to 20µm pitch.

With further reduction in solder volume to achieve finer pitches, the solder is expected to fully react into intermetallics, if not during chip-level assembly itself, then during subsequent process steps. Solid-liquid interdiffusion (SLID) bonding has been proposed and extensively researched as an alternative technology to form all-intermetallic joints with improved pitch scalability, power handling capability and thermal stability. However, the adoption of existing SLID technologies has been limited to date due to reliability concerns, notably related to voiding, and manufacturability and cost challenges due to low assembly throughput. This last technical challenge was addressed in the third research task with the design and demonstration of a void-free, manufacturable SLID technology. In the proposed metastable SLID technology, the Cu_6Sn_5 metastable phase was isolated using Ni diffusion barrier layers, enabling full conversion into void-free intermetallics with highest interdiffusion rates. Metastable SLID was demonstrated, for the first time, at pitches down to 20µm on Si and glass substrates, with superior shear strength of 90MPa, outstanding electromigration resistance at $10^5 A/cm^2$, good thermal stability after 1000h high temperature storage at 200°C and excellent thermomechanical reliability.

CHAPTER 1. INTRODUCTION

Transistor scaling has been aggressively pursued since the 1950's, resulting in rapid miniaturization and performance improvements of semiconductor devices such as microprocessors. However, transistor integration has recently slowed down, taking a longer time to reach the next technology node than predicted by Moore's Law. Electronic systems are concurrently increasing in complexity and require co-integration of many heterogeneous functions such as digital, analog and power, which cannot be achieved through silicon integration only. Semiconductor technologies are now reaching their fundamental limitations, forcing the semiconductor industry to rethink their system integration strategy and turn to packaging to meet the functional density requirements of emerging electronic systems. Georgia Tech is pioneering in System Scaling approach to address these challenges and enable complete heterogeneous system integration. High-density, ultra-thin, panel-scalable glass substrates are being pursued by Georgia Tech as the next generation packaging beyond organic laminates to start the "System Moore" era. As glass is bridging the interconnect gap with silicon, scaling of off-chip interconnections becomes critical to accommodate finer I/O pitches and higher densities, and reduce the interconnection length. This brings unprecedented performance, reliability and process challenges for interconnection and assembly technologies that are being addressed in this work.

1.1 System scaling trend in microelectronics packaging

High-performance computing systems have been driving advances in device, packaging and interconnection technologies over the last several decades to meet their

escalating performance, miniaturization and cost requirements. Transistor scaling, following Moore's Law, has been the basis of all these advances towards logic and memory integrated circuits (ICs) with increasing transistor densities and optimized performance. The System-on-Chip (SoC) technology, consisting of monolithic co-integration of digital, analog or RF circuitries in a single IC, was later pursued to further increase the functional density of electronic systems. However, transistor scaling has recently been slowing down, taking longer and longer time to go from node to node as the physical limitations of conventional CMOS technology are being reached and the complexity of integrating non-digital technologies in CMOS escalates. Further, there is no longer a cost reduction moving to the next node. These challenges in realizing Moore's Law's predictions have compelled the semiconductor industry to turn to packaging as the next platform for system integration [1]. The International Technology Roadmap for Semiconductor (ITRS) has recently modified their system integration roadmap to reflect this dual trend with "More of Moore" aiming at miniaturization of digital functions with new transistor concepts, and "More than Moore" targeting functional diversification on package with advances in packaging technologies and architectures [2].

Vertical stacking of thinned ICs with through-silicon vias (TSVs) was subsequently pursued to achieve even higher functional densities and integrate components at module level. This technology particularly gained importance with memory cubes, enabling a 3X jump in bandwidth between graphics processing units (GPUs) and memories, from 370 Gb/s to 1 Tb/s, while cutting power by a third by bringing processor and memories closer [3]. However, 3D-ICs still face design limitations in terms of thermal management and power delivery of logic IC [4]. The high cost of TSVs using Bosh DRIE process as well as

thermomechanical reliability concerns of Cu-plated TSVs have also limited wide adoption of 3D-ICs for system integration [5]. Further, “More than Moore” still relies on silicon integration and, therefore, inherently faces the same fundamental challenges as SoCs.

To bridge the gap between transistor scaling and system scaling, a new paradigm for system miniaturization and integration has been proposed by the 3D Systems Packaging Research Center at Georgia Tech with the pioneering System-on-Package (SoP) technology. In the SoP approach, heterogeneous functions are directly integrated on the package substrate. Packaging now becomes a key enabler to reduce the overall system cost and size, and, therefore, adds value to the system.

The SoP vision has rapidly gained momentum in high-performance computing, giving rise to advanced packaging technologies such as high-density 2.5D interposers. In 2.5D integration, a single, costly SoC die is split into multiple dies that can be fabricated with different, more cost-effective technology nodes. An interposer package with high-density wiring is then introduced for high-speed, high-bandwidth die-to-die communications. As an example is by AMD that applied the 2.5D architecture in their high-end graphic card Radeon R9 300 series, interconnecting Figi’s new GPUs and SK Hynix’s high-bandwidth memory (HBM) on a Si interposer with a 512 Gbits/s bandwidth [6]. 2.5D integration is also considered as the most cost-effective platform to co-integrate photonic ICs, optical fibers and digital chips [7]. Such digital-optical heterogeneous integration at package level is becoming more and more critical in the Datacom market with the emergence of cloud computing and optical communications to achieve ultra-high information densities at lower power consumption.

With such stringent requirements for off-chip interconnect density, 2.5D integration has, so far, heavily relied on the use of expensive and lossy silicon interposers. To address these cost and performance challenges, the Georgia Tech 3D System Packaging Research Center is pioneering ultra-thin, panel-scale glass substrates for advanced 2.5D integration, with Si-like wiring densities, improved electrical and reliability performances, at a cost point comparable to that of organic boards [8]. Glass also has a tailorable coefficient of thermal expansion between 3.8-9.8ppm/°C, giving design flexibility to balance chip- and board-level reliabilities. Large glass interposer packages can thus be directly assembled onto the mother boards without the need for an additional organic BGA package.

This new approach to system design utilizing advanced substrate technologies with interconnect pitches and densities close to matching on-chip wiring capability subsequently requires scaling of off-chip interconnection pitches with unprecedented performance and reliability requirements.

1.2 Scaling of off-chip interconnection technologies and emerging performance and reliability requirements

According to the ITRS roadmap, emerging high-performance applications are projected to drive system bandwidth requirements beyond 1 Tbits/s in the near future. This, in turn, brings the need for interposers with sub-5μm lithographic design rules and ultra-fine pitch off-chip interconnections, with I/O pitches down to 20μm by 2020.

Since the 1950's, interconnection and assembly technologies have continuously evolved from wire bonding to flip-chip to enable finer I/O pitches and higher densities, as illustrated in Fig. 1. Solder-based interconnections have become prevalent in fine-pitch

applications due to their suitable electrical properties, reliability, and ease of processability at low cost. Pitch scaling is, however, accompanied by a reduction in solder volume to prevent bridging. This aggravates thermomechanical strains in solder joints and, therefore, limits scalability of conventional C4 bumps to ~80µm pitch. The Cu pillar technology was later introduced for further pitch scaling, with Cu micro-bumps serving to increase the interconnection standoff height, thereby alleviating strains in the solder caps. To date, the Cu pillar technology has been demonstrated at pitches down to 40µm in production and 30µm in R&D, but faces several basic limitations hindering further scaling.

Technological evolution with pitch scaling has brought a continuous reduction in solder volume from 400µm-diameter C4 bumps down to 15-30µm solder heights in standard Cu pillars, and these are projected to reach about 10µm for 20µm-pitch interconnections. With this trend, intermetallics start contributing more significantly, to the point of eventually dominating the overall joints' composition, with the associated properties and reliability. Mechanical stresses intensify at the interface between residual solder and intermetallic to the level where they can potentially create micro-cracks resulting in joint failures. Managing these interfacial stresses has consequently become a major fundamental bottleneck to achieving reliable solder-based interconnections at ultra-fine pitches.

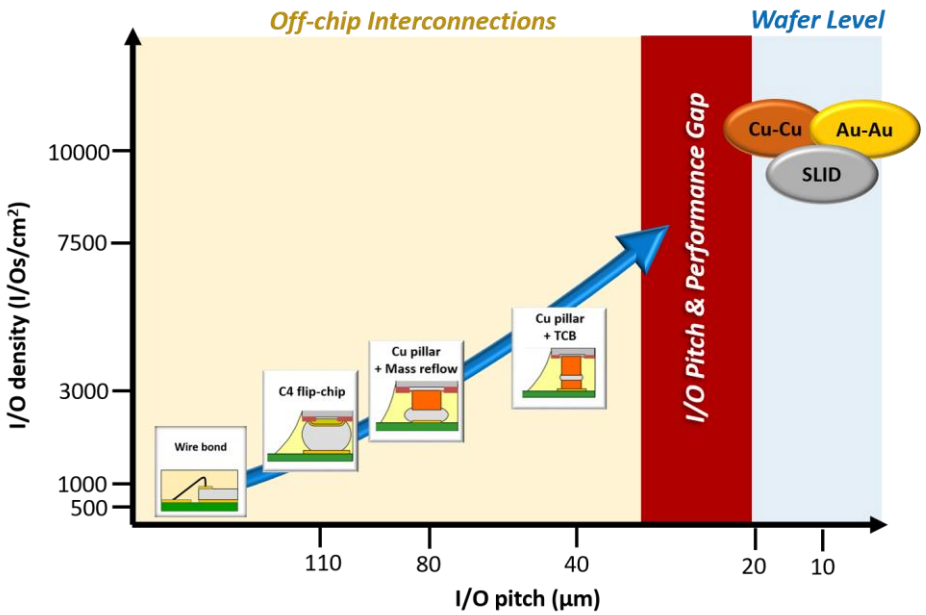


Figure 1. Evolution of interconnection technologies with pitch scaling.

In addition to the aforementioned reliability concerns, scaling of the Cu pillar technology is also inherently limited by the physical properties of solder alloys. Reduced interconnection diameters at such fine pitch result in increasing current densities as described in Fig. 2, up to 10^5A/cm^2 and above, and far exceeding the power-handling capability of Sn-based solder alloys. Further, increased power density brings significant heat flux within the package that overpowers the efficiency of existing thermal dissipation capability. Operating temperatures in emerging 2.5D packages are projected to rise to 100°C, near half the melting point of standard lead-free solders beyond which creep effects become extremely damaging to thermomechanical reliability [9].

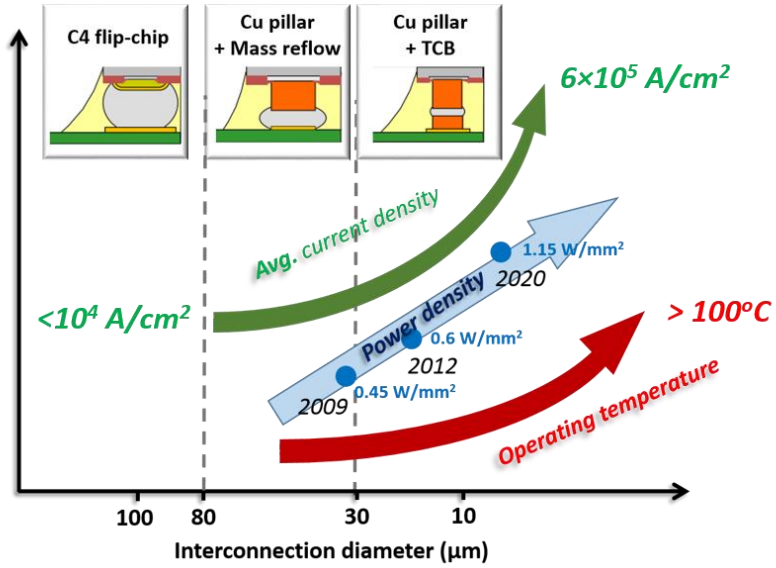


Figure 2. Emerging electrical and thermal requirements with pitch scaling.

Lastly, with such small amounts of solder, full conversion to intermetallics is almost unavoidable, if not during chip-level assembly, definitely during subsequent process steps. All-intermetallic interconnections formed by solid-liquid interdiffusion bonding (SLID) have recently been proposed as a natural evolution of conventional solder interconnections to extend their scalability to pitch sizes of 10-20µm [10]. In addition to their pitch scalability, intermetallics have high melting points giving high thermal stability and superior electromigration performance than solders. While promising and demonstrated in 3D-IC Si-Si bonding, SLID bonding technologies face many challenges for use in die-to-substrate applications, including long process times, costly bumping and assembly processes, and void formation degrading electrical, thermal and reliability performances.

Beyond solders, solid-state bonding technologies, such as direct Cu-Cu [11] or direct Au-Au bonding [12] have also been aggressively pursued and demonstrated at 10-

20µm pitch with suitable power handling capability and thermal stability. However, these wafer-level technologies face many manufacturability, reliability and cost challenges hindering their applicability to off-chip interconnections. New off-chip interconnection and assembly technologies are, therefore, required to bridge the I/O pitch and performance gap between package- and wafer-level interconnections shown in Fig. 1.

1.3 Research Objectives

Addressing the aforementioned critical needs, the primary objective of this research is to design, develop and demonstrate innovative and manufacturable off-chip solder-based interconnection and assembly technologies with pitch scalability < 20µm, standoff height < 15µm, thermal stability up to 200℃ and power-handling capability up to 10^5 A/cm^2. This is achieved by 1) scaling the conventional Cu pillar technology to 20µm pitch with a solder height of 10µm; and 2) demonstrate manufacturable, void-free SLID interconnections at 20µm pitch with power-handling capability and thermal stability beyond that of conventional solder-based technologies. The basic and fundamental properties, reliability and manufacturability objectives are reported in Table 1 and benchmarked against prior art.

Table 1. Research objectives beyond prior art and associated technical challenges.

<table>
<tr><th colspan="2" rowspan="2">Specification</th><th colspan="2">State of art</th><th rowspan="2">Research objectives</th><th rowspan="2">Challenges</th></tr>
<tr><th><u>Cu pillar</u></th><th><u>SLID</u></th></tr>
<tr><td colspan="2">Package configuration</td><td>Die-to-substrate</td><td>3D-ICs</td><td>Die-to-substrate</td><td rowspan="7">➢ Controlled intermetallic formation with reduced solder volume

➢ Manufacturable void-free SLID bonding for high performance</td></tr>
<tr><td colspan="2">I/O pith</td><td>35-100µm</td><td>10µm</td><td>20 µm</td></tr>
<tr><td colspan="2">Standoff height</td><td>25-35µm</td><td>10µm</td><td>10µm</td></tr>
<tr><td rowspan="2">Manufacturability</td><td>Bumping</td><td>Standard, low cost</td><td>Non-conventional</td><td>Standard, low cost</td></tr>
<tr><td>Assembly throughput</td><td>Reflow: > 40K UPH

TC-NCP: ~7s cycle time</td><td>20-40 mins transition time</td><td>SLID with < 1min transition time

2-step process with TC-NCP < 7s cycle time</td></tr>
<tr><td rowspan="3">Reliability</td><td>Power handling</td><td>8.3×10^3 A/cm^2</td><td>$1\text{-}5\times10^5$ A/cm^2</td><td>$1\text{-}5\times10^5$ A/cm^2</td></tr>
<tr><td>Shear strength</td><td>40-60 MPa</td><td>< 40MPa</td><td>> 70MPa</td></tr>
<tr><td>Thermomechanical</td><td colspan="3">JEDEC standard TCT at -40/125°C, 15min dwell time, 1 cycle/h</td></tr>
</table>

1.4 Technical Challenges

The key fundamental challenge in scaling the conventional Cu pillar technology to pitches below 20µm is to finely control interfacial reactions so as to mitigate interfacial stresses, aggravated by reduction in solder volume, to form reliable interconnections. Intermetallic formation and the subsequent joints' microstructure are governed by: a) the assembly process, in particular the dwell time of liquid phase reaction with accelerated interdiffusion rates; and b) the interconnection metallurgical system, in particular the surface metallurgy reacting with the solder. The specific challenges associated to both are detailed in the following subsections.

While the Cu pillar technology can be scaled to 20µm pitch, it cannot meet the power handling and thermal stability requirements of emerging high perfermance

computing applications. All-intermetallic interconnections have been proposed as a natural evolution of solder-based technologies owing to the superior current carrying capability and higher melting point of intermetallic compounds while benefitting from the ease of processability of solders. However, existing SLID bonding technologies face many challenges, including costly bumping processes, long assembly cycle times and reliability concerns due to voiding that limits their applicability to Si-Si bonding. The third challenge addressed in this work is to develop an ultra-fine pitch, manufacturable void-free SLID bonding technology for die-to-substrate applications.

1.4.1 Controlled intermetallic formation with reduced solder volume

1.4.1.1 Reaction control in fine-pitch assembly

Intermetallic formation in assembly is mainly governed by the time solder is involved in a liquid-phase reaction with the pad metallization. The resulting microstructure is determined by the balance of interdiffusion of multiple elements, dissolution and precipitation of intermetallics. Precise control of the reaction with shorter and shorter times in molten phase becomes more and more critical as the solder volume reduces to accommodate finer pitches. This cannot be achieved with standard reflow, and requires advanced assembly technologies with dynamic and precise control of the temperature in the solder throughout the process.

Thermocompression (TC) bonding with snap-cure pre-applied underfills has been identified as the most promising assembly technology for ultra-fine pitch interconnections, beyond conventional reflow. The significantly shorten assembly times improve pitch scalability with reduced solder height. In standard TC bonding, heat is generally applied

from the die side only, while the substrate is maintained at a constant temperature, constrained to 70-90℃ by the thermal stability on stage of current epoxy-based pre-applied underfill materials. This built temperature gradient also benefits warpage management, delamination of back end of line (BEOL) and assembly yield. Controlling the temperature distribution in the entire package is, therefore, a key advantage of TC-bonding. The temperature distribution is governed by heat transfer through the assembled package, which depends on the substrate design and materials. Consequently, TC bonding processes have to be customized for any given test vehicle to provide good control over interfacial reactions.

Further, advanced thermocompression bonding tools now enable heating rates of 200K/s and above for increased assembly throughput. The curing kinetics of pre-applied underfills is however highly sensitive to the heating rate, resulting in viscosity changes that can subsequently affect solder collapse and reliability. A systematic understanding of interactions between interconnection materials, package design, process and bonder is therefore critical to provide design guidelines for optimal assembly conditions, and future tool and materials development. This challenge is undertaken in unique approach I through modeling and design of TC-NCP processes on high-density, ultra-thin glass substrates.

1.4.1.2 Reaction control through interconnection metallurgical system

Pitch scaling of off-chip interconnections is accompanied by a dramatic reduction in solder volume, with less than 10μm solder heights expected in the near future. With this evolution, the volumetric contribution of intermetallics to the joints' overall composition becomes more and more significant, aggravating interfacial stresses between intermetallics

and residual solder, sometimes to the point of failure. Moreover, the properties of intermetallics then come to considerably affect electrical and thermal performance, as well as reliability. Fine control of interfacial reactions and intermetallic formation through optimization of the interconnection system has, therefore, become essential in achieving reliable interconnections. Surface finish metallurgies, as an inherent part of the interconnection system, play a critical role in defining the intermetallic compounds formed during the reaction and their growth rates.

So far, ENEPIG exhibited the best reliability performance of all existing finishes, granted by slow intermetallic formation rates in presence of Ni diffusion barriers. However, increasing concentrations of Pd and Au within joints as the solder volume decreases however raise serious reliability concerns due to escalating risks of Au embrittlement. The presence of Ni in large amounts in Cu pillar interconnection systems is also detrimental to their high-frequency performance.

Alternative finish technologies, such as immersion Sn or OSPs, face manufacturability and reliability challenges of their own in pitch scaling including poor wettability. A new class of Ni-free, ultra-thin surface finish metallurgies that provides ideal wettability and enables stable joints' microstructures is thus required to achieve reliable, ultra-short solder-based interconnections, potentially scalable to pitches below 30μm. This challenge is addressed in unique approach II by introducing the novel EPAG (Electroless Palladium Autocatalytic Gold) finish and optimizing its composition in Cu pillar interconnections with less than 10μm solder height.

1.4.2 Manufacturable void-free SLID bonding technology

All-intermetallic interconnections have been shown to successfully overcome the fundamental limitations of solders in electrical, thermal and reliability performances. Despite such outstanding performance, SLID bonding faces critical manufacturing and reliability challenges that needs to be addressed: 1) bumping manufacturability; 2) low assembly throughput from long transition times to form fully-stable intermetallics; 3) Kirkendall voiding degrading thermal and electromigration performances; and 4) thermomechanical reliability in assemblies with CTE mismatch, yielding high risks of failures in ultra low-K dielectrics in presence of stiff intermetallic joints. Although several studies have demonstrated that SLID interconnections can be formed within 1min by thermocompression bonding, the joints' composition was still not completely stabilized [13]. Further phase transformation may consequently happen during subsequent high-temperature operations, raising reliability concerns. Void formation induced by volume shrinkage during intermetallics formation is also inevitable without a comprehensive design of the SLID system. Unique approach III addresses these challenges with modeling, design, demonstration and characterization of the proposed metastable SLID bonding technology.

1.5 Unique Approach addressing technical challenges

To realize the aforementioned objectives and address the technical challenges, a unique approach of co-design of the interconnection system and assembly process was undertaken and developed with a focus on control of interfacial reactions and microstructures. The first problem of extending existing Cu pillar technology to finer pitches requires two key innovations, I and II, focusing on controlling interfacial reactions trough design of assembly processes and surface metallurgies, respectively. The new

concept of metastable SLID bonding is then introduced as innovation III, to meet the thermal stability and power handling requirements of emerging high-performance systems. The research strategy is described in Fig. 3.

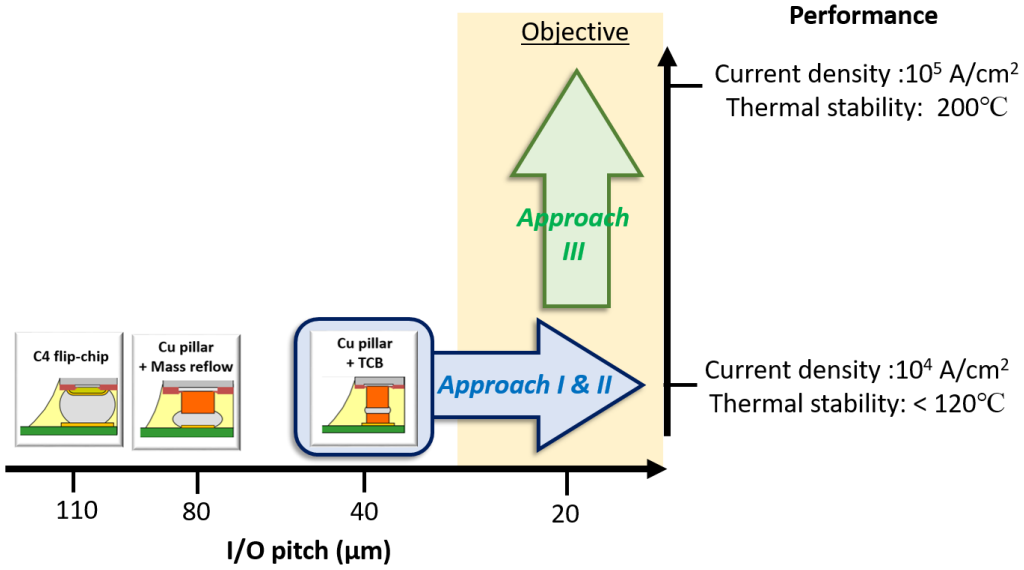


Figure 3. Roadmap of solder-based interconnection pitch scaling with GT's unique approaches

The three key innovations are as follows:

I) Ultra-fine pitch Cu pillar interconnections enabled by design and optimization of TC-NCP processes through finite element process modeling with consideration of interactions between tool, process, materials and package structure. TC-NCP is demonstrated, for the first time, with high-density glass substrates.

II) Ni-free Cu pillar interconnection system with ultra-thin electroless Pd – autocatalytic Au (EPAG) surface finish recently developed by Atotech GmbH to form ultra-short, reliable Cu pillar interconnections.

While innovations I and II enable pitch scaling with conventional solder-based interconnections, the thermal stability and power-handling capability are still limited by the fundamental material properties of solder alloys. These limitations are illustrated in Fig. 4, in which the low melting points of Sn-based solder alloys constrain maximum operating temperatures to 100-120℃, and the highly ductile mechanical properties reflect a high inclination for electromigration. The SLID bonding technology has been considered as one of the most promising technologies to satisfy emerging electrical and thermal requirements, owing to the ceramic-like high melting point and mechanical strength of intermetallics. Innovation III was pursued in this thesis to design and demonstrate a SLID technology with improved manufacturability and reliability that can be applied to die-to-substrate applications:

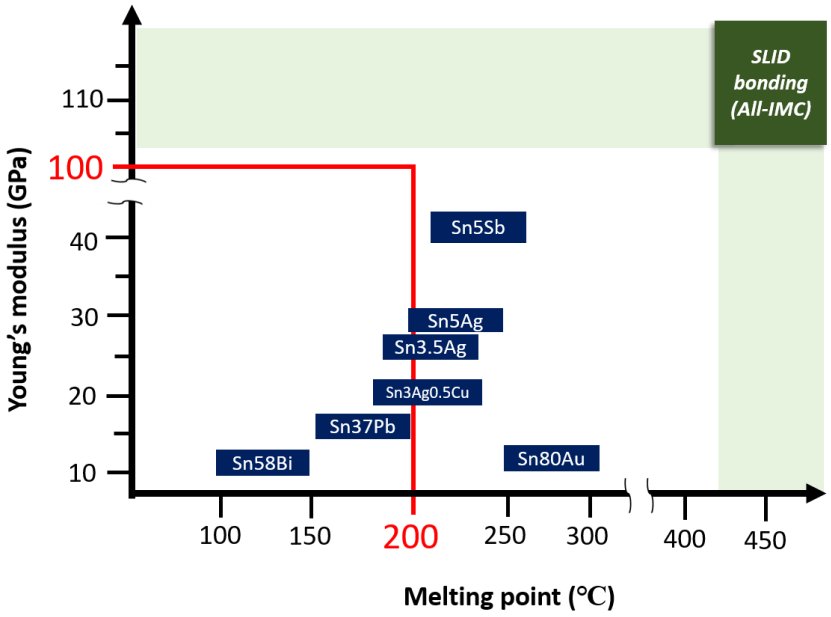


Figure 4. The melting point and Young's modulus of solder alloys vs. SLID bonded intermetallics.

III) Novel metastable SLID bonding concept introducing diffusion barrier layers to isolate the metastable Cu_6Sn_5 phase instead of the standard Cu_3Sn to achieve full conversion into intermetallics in less than a minute by reaction in liquid-phase only, and form void-free joints. The metastable SLID concept is compared to standard SLID in Fig. 5.

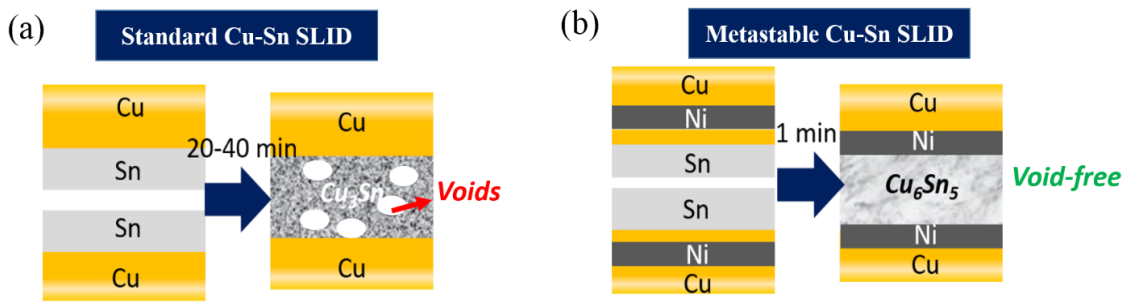


Figure 5. Schematics of standard vs. metastable SLID in the Cu-Sn system.

1.6 Research Tasks

The research tasks defined to address the three aforementioned technical challenges are summarized in Table 2, and detailed below. These research tasks individually relate to elemental technologies of off-chip interconnections: 1) advanced assembly processes and their manufacturing challenges; 2) surface finish metallurgy to control interfacial reactions and subsequent joints' microstructure; and 3) novel SLID interconnection system design. This work, therefore, provides a comprehensive study defining the next solder-based interconnection technology for high-performance applications.

Table 2. Research tasks vs. technical challenges.

Challenges	Tasks
1. Reaction control in fine-pitch assembly	1. Modeling, design and demonstration of TC-NCP for controlled reaction at fine pitch
2. Reaction control through interconnection metallurgical system	2. Optimization of interconnection system for reliable, ultra-short Cu pillar interconnections
3. Manufacturable, void-free SLID bonding technology	3. Modeling, design and demonstration of metastable SLID bonding at 20μm pitch

1.6.1 Modeling, design and demonstration of TC-NCP for controlled reaction at fine pitch

The objective of this task is to gain a fundamental understanding of thermocompression bonding with pre-applied underfill in order to control the solder collapse and interfacial reaction through less than 5s melting time of solder. The ultimate goal is to provide the design guidelines for ultra-fine pitch assembly, also contributing to the works in research task 2 and 3.

Finite element thermal modeling of a full package was first pursued to capture the effect of the substrate electrical design on heat transfer during bonding, as well as interactions between package and bonding tool. The calculated temperature gradient during actual bonding trials were then implemented as inputs of a second coupled-field model, in which the real-time stress and temperature evolution could be solved stepwise. The dependence of the curing kinetics of snap-cure pre-applied underfills on the heating rate in bonding was also considered and discussed. An empirical parametric study varying

substrate core material and thickness was carried out to validate the modeling results. Guidelines for underfill and TC process co-design were finally extracted for 3D-IC and die-to-package applications, considering current and next-generation interconnection technologies. The achievements related to this task are reported in Chapter 3, concluding with a design methodology applied to define the assembly processes used in Tasks 2 and 3.

1.6.2 Optimization of interconnection system for reliable, ultra-short Cu pillar interconnections

This task aims at demonstrating Cu pillar interconnections with less than 10µm solder height for potential scaling of the technology to finer pitches than achievable today. This task is carried out by optimizing the interconnection system with a focus on surface finish metallurgy and elimination of Ni, to finely control intermetallic formation, and subsequently the joints' composition, performance and reliability. Novel electroless Pd (EP) and EPAG surface finishes were introduced to address microstructural challenges at reduced solder volume, such as gold embrittlement and increased interfacial stresses. With thicknesses in the 50-150nm range, these finishes enable a gap loss between traces of less than 5% and are therefore compatible with advanced high-density packages with sub-5µm lithographic design rules [14]. Improved insertion losses |S21| at 67 GHz by 1 dB were also achieved with these novel finishes [15]. Although these technologies have already been demonstrated with wire bonding and BGA interconnections with promising results, this work is the first study with Cu pillars, 30µm in diameter, 10µm in height, and with a 10µm solder cap. With such limited solder volume, Pd and Au concentrations within the solder joints are critical due to risks of gold embrittlement.

A comprehensive study of EP and EPAG surface finishes was performed in this task with variations in surface finish composition considering Pd and Au thicknesses ranging from 50-100nm and 0-50nm, respectively. Wettability, interfacial reactions through high-temperature storage at 150℃, bond strength and thermomechanical reliability of ultra-short Cu pillar interconnections formed on all surfaces were evaluated, analyzed and compared to the performance of standard ENEPIG finish. An optimized composition of EPAG was finally derived, exceeding the performance of ENEPIG finish in all aspects, and enabling, for the first time, reliable Cu pillar interconnections less than 20µm in standoff height. The detailed analysis and fundamental discussion is described in Chapter 4.

1.6.3 Modelling, design and demonstration of metastable SLID bonding at 20µm pitch

The objective of this task is to design from first principle, demonstrate and characterize a new solder-based interconnection technology going beyond the fundamental limitations of standard Cu pillars by forming all-intermetallic joints. The proposed metastable SLID technology addresses the bottlenecks of standard SLID systems by targeting the Cu_6Sn_5 intermetallic as the final phase instead of the usual Cu_3Sn. This is accomplished by introducing double-sided Ni(P) barrier layers that block the Cu source and suppress formation of Cu_3Sn. Full transition to Cu_6Sn_5 can be completely achieved through liquid-phase reaction with high throughput, while eliminating the subsequent solid-phase transition from Cu_6Sn_5 to Cu_3Sn. The key advantages of this technology are: a) high-throughput assembly compatible with standard thermocompression bonding tools, materials and processes; b) ultra-thin (less than 5µm) bonding layers to prevent bridging at

fine pitch; c) higher thermal stability and electromigration resistance compared to traditional solder-based interconnections; and d) better thermomechanical reliability than state-of-the-art SLID technologies with lower standoff heights.

Finite element modeling was first used to predict interfacial stresses and strains to design the interconnection material stack and geometry for improved reliability. Theoretical diffusion and kinetic models were used to optimize the thickness of the Ni barriers, the alternate Cu/Sn/Cu stack-up, as well as the thermocompression bonding conditions. Based on aforementioned designs, an ultra-thin connecting layer, less than 5μm in thickness and solely composed of Cu_6Sn_5, was achieved through high-throughput thermocompression bonding with a 3s dwell time at 260℃. The bonded metastable SLID assemblies were then subjected to 10X reflow and 200℃ high temperature storage test for thermal stability, die-shear test, as well as electromigration test under high current density of 10^5 A/cm^2 at 150℃ for power-handling capability. Eventually, the metastable SLID bonding was demonstrated for thermomechanical reliability with 100μm-thick glass substrates, and 20μm pitch with chip-to-substrate configuration. The design, bumping and assembly, and reliability evaluation of metastable SLID bonding are detailed in Chapter 5, 6, and 7, respectively.

CHAPTER 2. LITERATURE REVIEW

This chapter begins with the evolution of electronic packaging architectures that has been driving the innovation of off-chip interconnections technologies. With the trend of moving to either single-chip packaging with large die such as mobile application or multi-chip packaging for high performance computing, the studies of chip-package interaction have gained growing attentions. This chapter will thus also review some important thermomechanical concerns surrounded the off-chip interconnections, and those critical items will then be taken into account when designing the off-chip interconnections in this thesis. The focus of this chapter will then be narrowed down to the advanced materials developed or being in R&D to addressing the challenges of off-chip interconnection system below 35μm pitch. The intermetallics growth control with different surface finishes will first be discussed with a solder height of 15-25μm. Then, with further reduced solder height below 10μm, all-intermetallics joints with novel SLID systems will be reviewed. Finally, the advanced material section will be ended with some recent activities and facing challenges of direct Cu-to-Cu interconnections without solder. Besides of the materials of interconnection system, some emerging assembly technologies for enhanced throughput at fine pitch will be covered in the last section.

2.1 The transition of packaging architecture

Modern electronic packagings could be described back to 1964, when the classy dual-in-line package (DIP) was invented with a 14 pins leadframe, in which the wire bonding was adapted to connect die to leadframe and the through-hole soldering or sockets were used for mounting the packages on printed circuit boards (PCBs). Driven by the escalating I/Os of the microprocessor, quad-in-line (QIL) or pin-grid-array (PGA) package could be considered as the descendants of DIP for pursing higher connection density. Being

well known as a high reliability platform, the low temperature co-fired ceramic (LTCC) pin-grid array (PGA) has still been adapted by AMD Phenom X4 processors, which is currently market available. Pioneered by IBM in 1980s, surface mount technology (SMT) was introduced to replace the through-hole soldering with the advantages of higher component density, higher connection density, and double side assembly on PCBs at lower cost. This move to SMT arose tremendous technical changes, including the metallization on Cu pads [16], the design of solder mask openings [17, 18], the studies on Sn37Pb solder [19], and the new assembly process such as solder paste stencil printing and reflow, which have been widely used till now. New package architectures were designed for accommodating this transition such as quad-flat package (QFP), dual flat no-lead (DFN), and quad-flat no lead (QFN). For high end application, the price of LTCC-PGA package tremendously increased for I/Os over 100s or pitch less than 1.25mm, since a high temperature and pressure brazing method was required to attach the pin on substrate metallization [20]. As the solution, in 1997, Pentium II microprocessor announced by Intel was the first high-end package that applies the ball grid array (BGA) package, in which a low cost solder ball array formed by stencil printing or solder ball plant was adapted in replace of costly pin in PGA. According to the statistics in 2013, flatpack/chip carrier (FP/CC), such as QFP, stands on the highest in demand within all the package types with a shipment of 50.9 billions units, and the BGA-typed packages hold 32.3 billions of units [21].

The increase of I/Os and transition of package architecture also affected the technologies of off-chip interconnections. Though wire bonding is a well-established process with high reliability and flexibility, it indeed has faced lots of physical limitations

when being adapted by new packaging architecture. The maximum I/Os is constrained by the active surface of chips, the extended wires increase the risk of coupling through molding, and the penalties of power, latency, and bandwidth caused by the long wires makes wire bonding inappropriate to high performance application. To extend the connectivity from peripheral area to all the active surface of die, the flip-chip with controlled collapse chip connection (C4) was developed by IBM, beginning from 1970s. While the Fig. 6 clearly shows the limitations of wire bonding [22], some statistics were also provided by Motorola in 1994 that indicated a 400% increment in interconnection density, a one third resistance reduction and a one eight inductance reduction being achieved by replacing wire bonding with flip-chip C4 [23]. Fig. 7 shows the structure of the first C4 design with Sn95Pb solder. With a multiple-layered under bump metallization (UBM), composed of Ti-Cr/Cu/Ni/Au, this technology sustained the off-chip interconnections scaling strain for decades, even the solder composition had been shifted from Sn95Pb, Sn37Pb, to lead-free solder.

However, beginning from the past 10 years, the scalability of C4 below 80μm pitch has been challenged due to the aggravating thermomechanical strains with continuously reducing solder height and some severe electromigration concerns [24]. The Cu microbump (Cu pillar) technology was then introduced with a 17-25μm-thick Cu column that enables enough standoff height for mechanical compliance [25] and current redistribution against electromigration [26]. From the manufacturing point of view, this transition is also beneficial by replacing costly UBM with relatively simple electrolytic bumping process. To date, the Cu pillar technology has been demonstrated at pitches down to 40μm in production and 30μm in R&D. Fig. 8 shows the 2.5D integration produced by

Xilinx in 2011, using 45μm pitch Cu microbumps to connect 28nm Virtex-7 SSIT chip on 100μm-thick Si interposer [27].

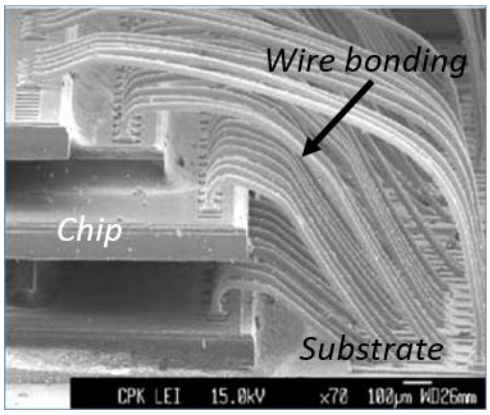


Figure 6. Wire-bonded 3D-ICs memory [22].

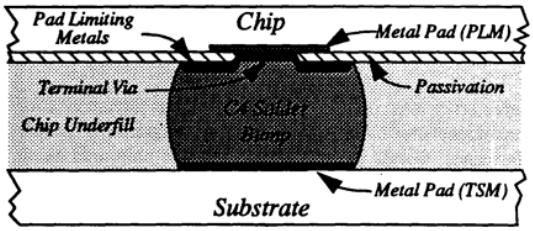


Figure 7. Schematic of the C4 solder bump with Sn95Pb solder [23].

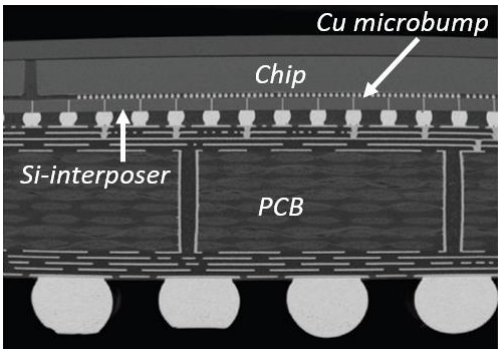


Figure 8. 2.5D integration with Cu microbump technology [27]

Lately, multi-chip package or multi-chip module (MCM) has started taking the market of single-chip module for high performance server system, owing to the advantages of high power efficiency, short routings, more aggressive design rule and higher functional density. This type of architecture includes the 3D-ICs, 2.5D interposer, 3D package-on-package (PoP) and so on. 3D-ICs was once considered as the most promising way to go

beyond the Moore's Law; however, the power delivery, thermal management and the constrained capability of signal integration have drawn the limitation of this technology. 2.5D integration counts on a high density interposer to maximize the bandwidth between modules, expecting to reach same electrical performance as 3D-ICs but with lower cost and higher flexibility. As the key enabler of 2.5D integration, 3D System Packaging Research Center in Georgia Institute of Technology has been dedicated in large panel glass interposer development. A six metal layered 2.5D glass interposer with minimum 3μm RDL lithography and 20μm microvia pitch has been demonstrate in 2016 [28].

Recently, Fan-out wafer level packages (FO-WLP) are introduced as a break-through architecture of entire semiconductor industry due to its size, cost, performance and reliability benefits compared to traditional flip-chip and wire bond packages. The driving factors for the implementation of FO-WLP technology are the low packaging and test costs, excellent electrical and thermal performance, improved reliability compared to WLP, and the potential for heterogeneous integration. One of the key attractions of FO-WLP is the simplified process flow benefited from the architecture without costly through interposer vias. A major trend in fan-out packaging is the move to large panel formats, so-called fan-out panel level packaging (FO-PLP) to increase productivity and further reduce cost. FO-PLP technologies can be broadly classified into 1) laminate embedded solutions, such as Imbera's Integrated Module Board (IMB) [29], AT&S's Embedded Components Packaging (ECP) [30], and ASE's advanced – Embedded Assembly Solution Integration (a-EASI) [31]; 2) panel fan-out solutions, including Amkor/J-Devices Wide Strip Panel Fan-out Package (WFOP) [32], PTI's panel-scale molded fan-out, and 3) chip-last PLP, such as ASE's coreless embedded trace approach. The process flow of chip-first ASE's –

EASI and chip-last ASE's process coreless embedded trace approach are showed in Fig. 9(a) and Fig. 9(b), respectively. Even the chip-last architecture has been proposed to achieve fine-pitch chip-to-package interconnections by replacing conventional off-chip Cu microbumps with Cu routings through semi-additive process (SAP), the yield lost caused by known-good-die (KGD) indeed limits the profits gained from process simplification. As the result, chip-last FO-PLP was projected to be widely adapted as a more mature architecture, in which a continuing need to improve I/O density, high frequency performance, yield and cost beyond existing Cu microbump technology is still a key enabler of FO-PLP.

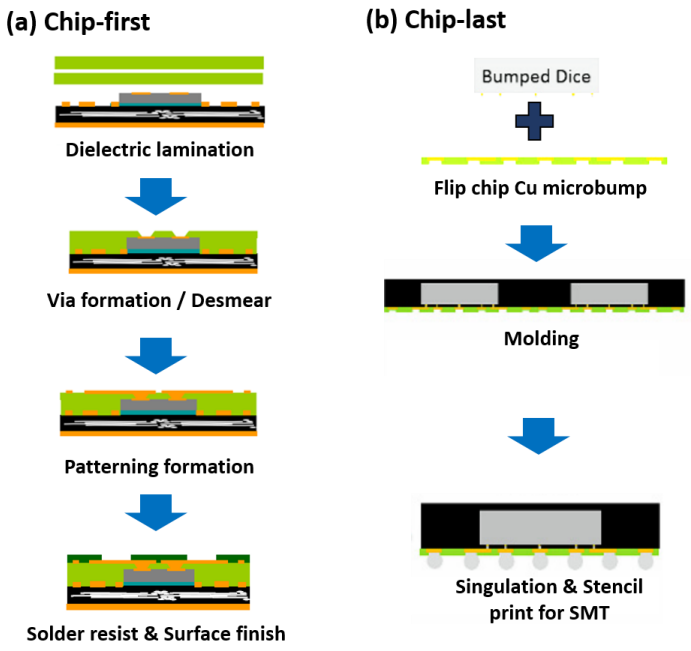


Figure 9. Process flows of (a) chip-first, and (b) chip-last FO-PLP.

2.2 Advances in material for fine pitch off-chip interconnections

2.2.1 Intermetallics control at fine pitch with emerging surface finish technologies

Surface finish, applied as a protective layer on exposed substrate copper metallizations, is involved in the interfacial reaction with solder during bonding, conditioning overall joints' strength and reliability. Surface finish technologies have been studied for decades to improve the performance of off-chip interconnections. Established technologies include Organic Solderability Preservatives (OSPs), Immersion Sn (ImSn), Immersion Ag (ImAg), Electroless Ni – Immersion Au (ENIG), Electroless Ni – Electroless Pd – Immersion Au (ENEPIG), and Direct Immersion Gold (DIG).

Nickel-based metallic finishes such as ENIG and ENEPIG are today industry's technologies of choice, owing to their superior properties such as ideal solder wettability, excellent joint strength and reliability performance. Solder joint failures were however experienced with ENIG finish, known as black pad defects as a result of galvanic hyperactive corrosion of the electroless Ni by the Au plating bath [33, 34]. This defect was also found highly dependent on design of Cu features, limiting scalability to large substrate panel sizes [35]. First introduced to solve ENIG's black pad issue, ENEPIG has soon become standard in high-end applications for its unprecedented reliability enhancements, despite its relatively high cost [36, 37]. Recently, the scalability of ENEPIG to a solder height lower than 10µm has been challenged due to the high inclination of precipitating Pd-Sn intermetallics. Benchmarking the reliability over 1000 thermal cycles with Ni/Au surface, ENEPIG was confirmed to fail within 250 cycles [38]. With those well-established surface finishes of ENIG and ENEPIG, some modifications based on existing stackup have been conducted for fine-pitch off-chip interconnections. A new stackup with 100nm-thick

Ni and 400nm-thick Au was demonstrated with Cu microbump without Ni barrier layer, and a preferable Cu-Sn intermetallic was formed without Au embrittlement or brittle Ni-Sn intermetallics [39]. However, the challenge came from fine-pitch wiring, with sub-10μm gaps between traces could not be addressed simply by thinning the Ni thickness. Announced by Atotech GmbH, thin ENEPIG, with reduced nickel thicknesses down to 0.15μm, was recently proposed to address this challenge but is still facing issues of extraneous plating as well as additional risks of copper corrosion [15]. With all the limitations found recently with ENEPIG and ENIG, the requirements of desirable surface finish with reduced solder volume are: 1) Ni-free surface finish for preventing extraneous plating; 2) Metallization that forms relatively durable Cu-Sn intermetallics without Au embrittlement. However, the existing Ni-free solutions, such as OSP, ImSn, ImAg and DIG face limitations of their own, as explained below.

The OSP technology is widely used in printed circuit boards (PCBs) and Ball Grid Array (BGA) packages due to its low cost. The organic compounds of OSPs are based on aza-aromatic bicyclic molecules, which form organometallic compounds with Cu to provide effective protection against corrosion. Superior drop-test reliability of BGA packages was reported with OSP as compared to ENIG finish [40]. This result was attributed to discrepancies in interconnection compositions, with Cu_6Sn_5 formed with OSP but $(Cu_x,Ni_{1-x})_6Sn_5$ with ENIG, resulting from cross diffusion of Cu from the substrate metallization. The morphology transition from scallop-shaped Cu_6Sn_5 to needle-shaped $(Cu_x,Ni_{1-x})_6Sn_5$ [41, 42] degrades the drop performance due to higher stress concentrations at the tip of needle-shaped intermetallics. In 2015, Qualcomm proposed to apply OSP on off-chip interconnections as a solution of lower cost, in which the as-bonded quality was

highly demanding on the fluxing agent in NCP material [43]. Generally, OSP finish needs to be completely dissolved in assembly to enable proper wetting of the solder onto the Cu pads. This is typically achieved by use of aggressive fluxing agents, containing organic or inorganic acids. In advanced fine-pitch assembly with pre-applied underfill materials, the fluxing action is designed as an integral part of the cross-linking network, requiring more neutral fluxing agents that fail to react with the OSP layer. While higher flux concentrations may improve its effectiveness, it drastically slows down underfill curing kinetics, subsequently degrading assembly throughput, increases void occurrences, reduces the glass transition temperature (Tg) of the cured underfill, and degrades the material's shelf life [44, 45]. Although strategies to facilitate OSP removal are being explored, such as the use of Ar/O2 microwave plasma [46], OSP is generally considered not compatible with modern TC-NCP processes. In addition, application of OSP at chip level is comparatively limited due to significant intermetallic growth in the absence of a diffusion barrier. A thick Cu_6Sn_5 layer indeed forms at a fast rate from the Cu-OSP surface, and is always accompanied by a thin layer of Cu_3Sn underneath. Kirkendall voids have been reported to form in Cu_3Sn due to differential diffusion fluxes of Cu and Sn, causing brittle fractures in the joints and lowering their shear strength to below 40MPa [47, 48].

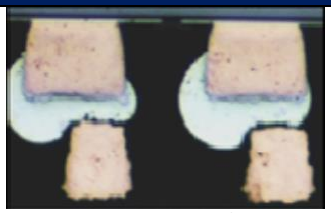
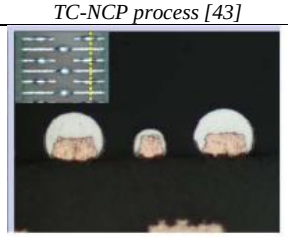
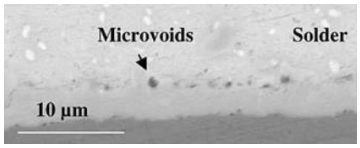
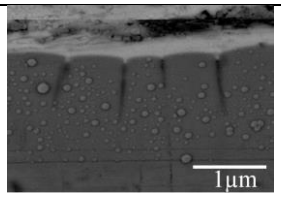
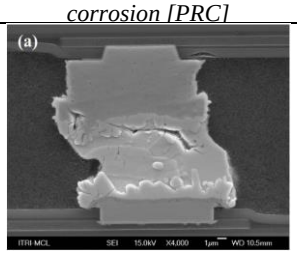
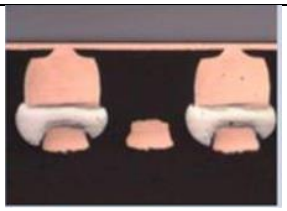
Immersion Sn was developed in the 90's as a low-cost surface finish alternative with improved wettability over OSP [49, 50]. However, wettability of ImSn was found to be highly variable depending on deposition thickness, environmental temperature and moisture. In 1994, AT&T Bell Laboratories reported significant degradation of ImSn solderability after a week of exposure at 30°C/90% RH and 60°C/85% RH caused by SnO_x growth on the surface [49]. Solderability of 1µm-thick ImSn also dramatically worsened

by 6h of pre-conditioning at 155℃ due to excessive consumption of Sn and intermetallics formation [50]. In current TC-NCP processes on organic substrates, a minimum 2h pre-bake at 120℃ is required to prevent voiding in underfill, thereby presenting non-negligible risks of solderability degradation. Pitch scalability of ImSn is also compromised by tin whiskers growth, up to 15μm in length [51]. To address aforementioned challenges, additives in the ImSn plating chemistry as well as a post-treatment have been implemented to limit whiskers formation and oxidation, respectively [52]. A minimum 0.3μm-thick layer of unreacted Sn after pre-conditioning was recommended by Atotech GmbH for sufficient solderability. In 2014, Amkor proposed the solder coat technology in replace of gold-based surface finish. However, except of having same challenges of ImSn, a five-time difference of coated tin thickness on neighboring traces was found [53]. Similar to ImSn, ImAg was introduced as an alternative but with extended shelf life. ImAg shows improved wettability than OSP and ImSn, especially after temperature-humidity storage. However, a high potential difference between Cu and Ag makes ImAg surface vulnerable to galvanic corrosion. And the migration of silver atoms through temperature humidity-bias (THB) accelerated test can cause bridging between fine routings [54, 55]. With as-bonded samples, the microvoids caused by the organic additive in ImAg plating chemical limit the bonding strength of formed joints.

DIG surface finish is a relatively new technology, driven by the demanding requirement of dimensional definition in RF applications. With a thickness of 50nm, DIG surface shows outstanding electrical performance, without being compromised by skin effect [56]. Recently, Altera has demonstrated the compatibility of DIG surface to TC-NCP process at 40μm pitch bond-on-trace (BOT) design [57]. The deposition mechanism

includes first an immersion gold process, followed by an electroless gold process, which requires a fine control within small process window in order to achieve porosity-free ultra-thin coating.

Table 3. Pros and cons of existing surface finish technologies

	Pros	Cons	
OSP	Pitch scalability, low cost, high drop-test reliability of BGA	Compatibility with TC-NCP process, IMCs growth	 *Non-wetting with OSP surface through TC-NCP process [43]*
ImSn/ Solder coat	Ideal as-deposited wettability, low cost	Surface oxidation, thermal stability, IMCs growth	 *Non-uniformity of solder coat [53]*
ImAg	Improved stability than ImSn, low cost	Worse wettability than Au-based and ImSn, migration, corrosion, microvoids	 *Microvoids with ImAg in interface [54, 55]*
ENIG	Ideal wettability and bonding strength	Corrosion, pitch scalability	 *Black pad induced by hyperactive corrosion [PRC]*
ENEPIG	Ideal wettability and bonding strength, improved reliability	Pitch scalability, high cost	 *Crack after 250 TCT with ENEPIG [38]*
DIG	Ideal wettability, improved electrical performance	Porosity, IMCs growth, immature technology	 *Demonstration of TC-NCP on DIG surface [57]*

2.2.2 Novel interconnection technologies for fine-pitch

As introduced in Chapter 1, requirements for the next node of interconnection technologies include: 1) scalability to 20μm pitch and below, 2) ultra-short bumps with less than 10μm standoff height for improved electrical performance, 3) thin connecting layer to limit risks of bridging, 4) high thermal stability over 200℃, 5) high power-handling capability with over 10^5A/cm^2 current densities, 6) compatibility with high-throughput TC-NCP processes. Conventional solder-based interconnections fail to satisfy these needs due to their relatively low melting points, and poor current-carrying capability limited to 10^4A/cm^2 [58].

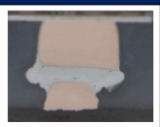
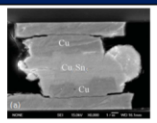
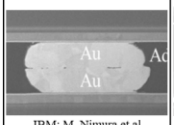
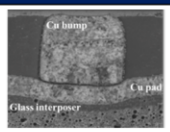
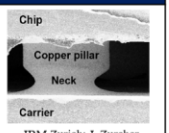
Complete elimination of solders is perceived as the ultimate solution to address this grand challenge, and has consequently been driving solid-state bonding technologies. Au-Au interconnections (GGI) were established by both thermocompression and ultrasonic bonding, but their applicability is limited by the high cost of Au and power handling capability, despite their excellent overall performance [59, 60]. Copper, on the other hand, is relatively inexpensive, and has outstanding electrical and thermal conductivities, thermal stability, current-carrying capability, high-frequency performance and is compatible with standard back-end-of-line (BEOL) infrastructures [61, 62]. However, direct Cu-Cu bonding faces three fundamental challenges degrading manufacturability: 1) oxidation, 2) relatively low diffusivity of Cu at reasonable bonding temperatures; and 3) low tolerance to non-coplanarities in the absence of a low-modulus molten phase. To improve manufacturability, GT-PRC recently pioneered low-temperature Cu interconnections, using ultra-thin Au-based metallic finishes to inhibit copper oxidation and form strong, reliable joints at temperatures below 200°C [63]. This technology, however, still

necessitates relatively high bonding loads with a nominal pressure in the 120-365MPa required to accommodate 3µm of non-coplanarities. The use of nanocopper inks to form all-Cu interconnections by capillary bridging was recently proposed by IBM Zurich to address this challenge [64]. Despite its potential, this sintering technology faces many limitations of its own, principally related to microstructural instabilities with retained porosity degrading bond strength, electromigration and thermal performances, limited manufacturability and high cost of Cu nanoparticles due to extensive surface treatment required to prevent oxidation [65, 66]. Novel interconnection solutions retaining the processability and cost effectiveness of solder-based approaches but with performance improvements are, therefore, highly desirable.

Diffusion soldering, or solid-liquid interdiffusion (SLID) bonding, aims at controlled formation of all-intermetallic joints by introducing multi-layered bumps with 2 basic components: a high-melting point metal such as Ag, Au or Cu, and a low-melting element such as In or Sn acting as wetting layer. SLID bonding, therefore, comes as a natural technology evolution to extend applicability of solders to finer pitches with minimum changes in infrastructures and processes. Other than their superior pitch scalability, SLID interconnections benefit from their excellent thermal stability due to the generally high melting points of intermetallics while maintaining same process temperature than solders, and outstanding power-handling capability with current densities exceeding the capability of solders. Owing to these properties, diffusion soldering was identified as a key technology for high-temperature die-attachment of vertical Si or SiC power devices in high-power modules and has consequently been extensively researched in the last decade in various metallurgical systems [67]. Infineon, for instance, started implementation of Cu-

Sn SLID interconnections in their IGBT (insulated gate bipolar transistor) modules in 2012 with a confirmed 30-40X increase in power cycling reliability [68]. More recently, diffusion soldering has been aggressively pursued in microelectronics for fine-pitch, high current-density interconnections. In 2015, TSMC reported the electromigration "immortality" of Cu-Sn SLID interconnections with over 9000h at a current density of 1.4-2.1×10^5 A/cm^2 and 160-170°C. This year, IMEC demonstrated Cu-Sn SLID interconnections at 10μm pitch for DRAM memory devices stacking, using damascene processes for bumping and embedding the bumps in polymer at wafer level [69]. Table. 4 compares the properties of existing fine-pitch interconnection technologies, including Cu pillar, SLID and solid-state bonding as well as emerging sintering technologies.

Table 4. Properties of existing fine-pitch interconnection technologies

	Cu microbumps	SLID bonding	Solid-state bonding			Nano-Cu sintering
			Au-Au bonding for 3D-IC	Cu-Cu for 3D-IC	Cu bonding with surface finish	
	 Amkor: J. Park et al., 2015.	 ITRI: J.Y. Chiang et al., 2012.	 IBM: M. Nimura et al., 2013.	 Z. Liu, et al., 2015.	 PRC: N. Shahane et al, 2015.	 IBM Zurich: J. Zurcher, et al., 2015.
Pitch	>40μm	15-20μm	<30μm	<10μm	<30μm	> 150μm
Height	30-45μm	<10μm	<10μm	<4μm	10-15μm	~100μm
Reliability	• Max. 10^4 A/cm^2 current density • ~230°C melting point	• >10^5 A/cm^2 current density • 450-800°C melting point	• 10^4 A/cm^2 current density • 1064°C melting point	• >10^6 A/cm^2 current density • 1085°C melting point	• >10^6 A/cm^2 current density • 1085°C melting point	• 5-8 MPa shear strength • 26 mΩ per interconnection
Bumping	Electroplating	Electroplating/ E-beam	Electroplating E-Beam	Damascene	Electroplating	Dipping with nano-ink
Bonding temperature	230-260°C	180-260°C	>250°C	300-400°C post-annealing (UHV or Ar)	200-300°C	250°C
Bonding time	<1min	2-30min	10s-10min	30min	1-10min	1-5min
Pressure	3 MPa	4.7 MPa	2-5 MPa	Pressure less	100-365 MPa	Pressure less

Many metallurgical systems have been explored for diffusion soldering, such as Ag-In, Ag-Sn, Au-In, Au-Sn, and Ni-Sn, but most of these methods have been reported to

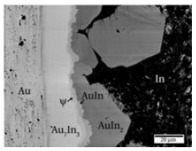
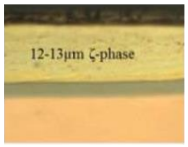
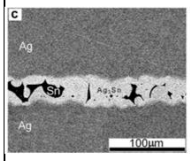
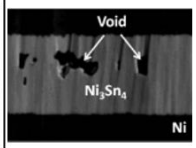
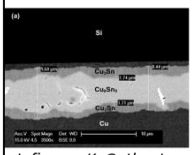
face insurmountable manufacturability and reliability challenges. The Ag-In system was particularly attractive for MEMS applications due to the low melting point of In (156℃), ideal for minimizing thermally-induced residual stresses and strains [70]. After assembly at 180°C for 40min, the joints, composed of both $AgIn_2$ and Ag_2In phases, exhibited a heterogeneous microstructure. The presence of $AgIn_2$ inherently limits the joints' thermal stability to less than 166^{o}C, its melting point [71]. An additional annealing step at 130℃ for 24h was proposed to fully convert $AgIn_2$ into Ag_2In and subsequently improve thermal stability, up to 695℃. Even higher thermal stability, up to 920℃, could be achieved with high-temperature annealing at 450℃ for 4h, shifting the joints' composition to the Ag solid solution phase. The Ag-In SLID system however faces specific reliability and manufacturability challenges, limiting its adoption. Poor adhesion between $AgIn_2$ and the sputtered Cr layer from the device under bump metallization (UBM) raises delamination concerns. High inclination of In oxidation also constrains the assembly process to use high vacuum in addition to prohibitory long bonding times. A promising stack-up addressing some of these challenges was recently proposed by UC-Irvine, in which Ag was deposited in excess on both bump and substrate sides for appropriate adhesion, and a thin additional Ag layer was plated on top of the In layer for protection against oxidation [72].

The Au-Sn system has also been intensively studied for high-temperature applications, benefitting from the high melting point (522°C) of the resulting phase (ξ, Au_5Sn). Limited by the eutectic Au 20wt%Sn composition, a temperature of 360℃ is required to facilitate the diffusion flux of Au into solder and isothermal solidification. A minimum required bonding time of 6min was reported to enable a shear strength higher than 60MPa [73]. Excessive thick Au layer was also found necessary to stabilize the

microstructure and solely retain the ξ phase through subsequent reflow or high-temperature storage as thermodynamically preferred phases, such as Cu_6Sn_5, Cu_3Sn, Ni_3Sn_4 or Ni_3Sn_2, can gradually emerge [74, 75].

The Cu-Sn system has emerged as the most promising candidate for SLID bonding in microelectronic applications as it's 5x faster transition rate comparing to Ni-Sn [76], and less than 4% volume shrinkage can be managed with Cu_6Sn_5, comparing to 11.3% of Ni_3Sn_4 and 9.1% with Ag_3Sn [77, 78]. In addition, Cu-Sn system is closest to current micro-bumps stack-up and can, therefore, reuse existing bumping infrastructures and processes as well as maintain bonding temperatures. The properties of the most common SLID systems are compared in Table 5.

Table 5. Properties of SLID bonding with different metallurgical systems

System	Ag-In	Au-Sn	Ag-Sn	Ni-Sn	Cu-Sn
Snapshot	 *B.J. Grummel, et al., 2013.*	 *SINTEF: A. Torleif et al., 2013*	 *J.F. Li, et al., 2010.*	 *H.Y. Chuang, et al., 2012.*	 *Infineon: K. Guth, et al., 2012.*
Bonding temperature	180-190°C	350-360°C	260°C	260°C	260°C
Bumping	E-beam	E-beam	Ag foil / Electroplating	Electroplating	Electroplating
Bonding time	15 min (under vacuum)	15min for 12μm	2min for 5μm	15-30min	15-30min
Pressure	3 MPa	4.7 MPa	2-5 MPa	2-5 MPa	< 3 MPa
Melting point	450-540 °C	450 °C	480°C	794.5 °C	638.4 °C
Volume shrinkage	-	AuSn: -12%	Ag_3Sn: -9.14%	Ni_3Sn_4: -11.3%	Cu_3Sn: -27.3% **Cu_6Sn_5: -3.9%**
Main Challenges	• Multiple phases • Indium oxidation • Delamination	• Cost • High bonding temp	• Cost • Deposition • Brittleness	• Low transition rate • Volume shrinkage	• Voids • Solid-state transition

Despite its many advantages, SLID bonding faces many challenges hindering its applicability in mass production, including long transition times governed by solid-state interfacial reactions, inherent void formation degrading the joints thermal performance and thermomechanical reliability, as well as limited manufacturability. So far, SLID bonding has mainly been implemented in CTE-matched Si-to-Si assemblies such as wafer-level or 3D IC applications [79]. Its use in substrate-level assembly is limited by the brittleness and stiffness of intermetallics, Kirkendall voiding [47] and shrinkage holes [80]. From manufacturability standpoint, SLID interconnections require a fine control of the bump initial composition with elemental layer deposition often using cost-intensive processes such as E-beam evaporation [76, 81]. Finally, SLID bonding generally requires long

transition times to achieve a single stable intermetallic phase, with 15 to 30 min of annealing time above the solder melting point, which drastically lowers assembly throughput [82, 83]. A new SLID bonding technology that enables formation of void-free interconnections with ultra-fast transition times and improved manufacturability is thus highly sought after by the semiconductor industry.

2.3 Developments of assembly process for fine-pitch off-chip interconnections

With the pitch scaling, solder bridging and massive intermallic growth have drown the limit of using the assembly process of mass reflow plus capillary underfill. A new assembly process, thermocompression bonding with nonconductive paste (TC-NCP), has been introduced to achieve improved solder collapse and intermallics control, and also as-bonded yield. Taking the Cu-Sn system for example, a ~3μm-thick Cu-Sn intermetallic from one single growing front would form after a standard reflow cycle with 260℃ peak temperature [84]. With a reduced solder height of 10μm or even less, such large ratio of intermetallics to unreacted solder would bring highly concentrated stress through the heterogeneous interface. With a relatively short melt period through TC-NCP, normally less than 5s, a superior intermetallic control can be achieved while keeping enough compliance gained from unreacted solder. With the solder collapse confinement benefiting from the pre-applied underfill materials, TC-NCP keeps driving attentions due to its potential of ultra-fine pitch applications, especially for 3D-ICs. For example, ITRI has demonstrated Si-to-Si interconnections at 20μm pitch with a 4μm Cu pillar and 4μm Sn cap through TC-NCP process [13]. In this year, IMEC has pushed this technology down to 10μm pitch by embedding the solder pillars into a non-cured polymer, followed by the chemical mechanical planarization (CMP) [85]. However, to be widely adapted to off-chip

interconnections, a basic understanding of thermocompression bonding processes and interactions between bonder, underfill and package design is critical to optimize assembly throughput and reliability, and provide guidelines for future development of interconnection materials and tools.

For next generation off-chip interconnections, a significant reduction of solder height is an inevitable transition, which causes the loss of high mechanical compliance gained from conventional Cu microbump. An aggravated stress releases in ultra-low dielectric constant (ULK) materials within the back-end-of-line (BEOL) of silicon processing, causing delamination issues. And an increased plastic strain within short solder cap damages the thermal fatigue lifetime of interconnections. Fundamental understanding of chip-package interactions (CPI) consequently became increasingly important. With the unique localized heating of TC-NCP process, a temperature gradient built between bonding heat and stage enables the substrate to be remained at lower temperature while reaching the melt point of solder. The stress or strain induced by mismatch in coefficients of thermal expansion (CTE) between silicon and high-density substrates, in particular laminates, can be significantly reduced. Global Foundries recently reported that the normal stress built in ULK layers could be reduced by approximately 85% with TC-NCP assembly as opposed to mass reflow [86], as showed in Fig. 10(a). In 2016, Shinko also found that the plastic strain in solder could be reduced by 25-30% as comparing to mass reflow, as showed in Fig. 10(b) [87].

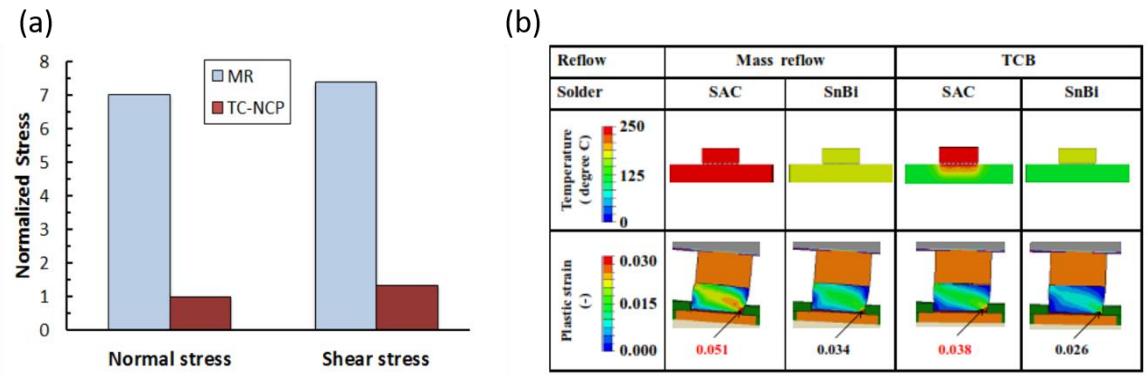


Figure 10. (a) Reduced stress in ULK-layer [86], and (b) reduced plastic strain in solder [87], benefited from thermocompression bonding.

Originated from the same root, the CTE-mismatch between die and substrate brings aggravated warpage concerns with the escalating trend of die and package thickness reduction to less than 100 and 300μm, respectively, and concurrent increase in package size. Fig. 11(a) shows the findings published by Amkor this year with conventional mass reflow process, in which a bump tearing and non-wet were caused by a crying warpage with a package size of 55mm × 55mm [88]. Unlike mass reflow which relies on isothermal heating, a thermal gradient established in the package in TC-NCP reduced thermal shrinkage. Through optimization of the force and thermal profiles, stage temperature and NCP material, post-assembly warpage can be finely controlled and minimized by managing the timing of coupling die and substrate, as showed in Fig. 11(b) [89]. Improved yield and reliability were consequently demonstrated with TC-NCP through unbiased highly accelerated stress test (uHAST), temperature cycling, and high-temperature storage (HTS) [43, 86].

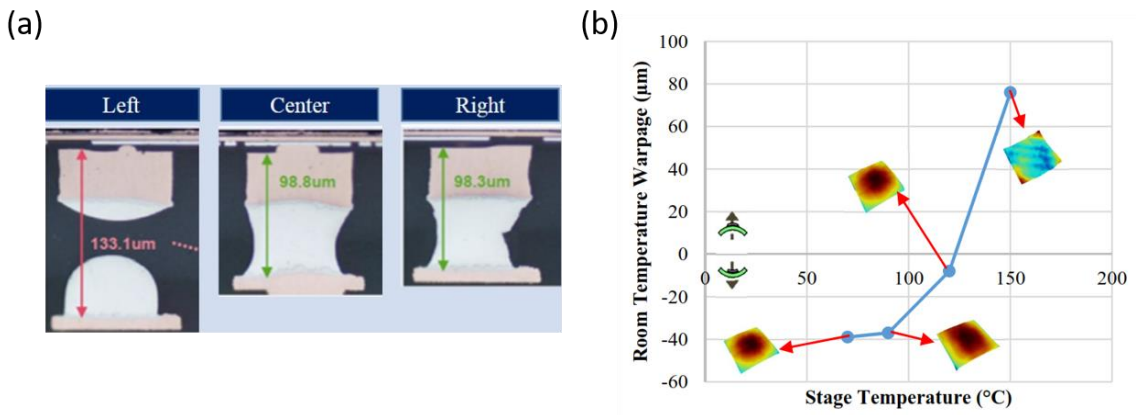


Figure 11. (a) The non-wet failure found with mass reflow process [88], and (b) the room temperature warpage as a function of stage temperature with thermocompression bonding [89].

In addition, with the view of assembly process flow, this transition from mass reflow plus capillary underfill to TC-NCP has also gained large momentum from the underfilling. Pitch scaling and corresponding reduction of die-to-substrate gap to below 50μm also introduces difficulties in flux cleaning and capillary underfilling. While recent research efforts have been made towards the use of plasma-assisted dry soldering to address the flux residue problem [90], capillary underfill (CUF) is fundamentally limiting by extended filling times with reduced gap and increased package sizes. The filling time is given by Equation 1:

$$t = \frac{3\eta L^2}{h\gamma \cos\theta} \tag{1}$$

where η is the underfill's viscosity, γ is the surface tension, θ is the contact angle, h is the die-to-substrate gap, and L is the package size. In addition, to maintain a maximum solder volume, pitch scaling is aggressively driving reduction of the interconnection gaps, causing slower liquid meniscus velocity of the underfill [91]. TC-NCP process successfully

addressed these challenges by using no-flow underfills, which was first developed in 1996 [44, 92]. No-flow underfills are applied on substrate or wafer prior to assembly, and cure during the bonding process itself. As a result, the composition of these pre-applied materials is more complex than that of capillary underfills, including the resin, hardener and inorganic fillers, but also a catalyst and fluxing agent to enable self-fluxing and snap-cure in bonding. Significantly simplify the assembly process flow, as shown in Fig. 12, making it an attractive solution for fine-pitch applications.

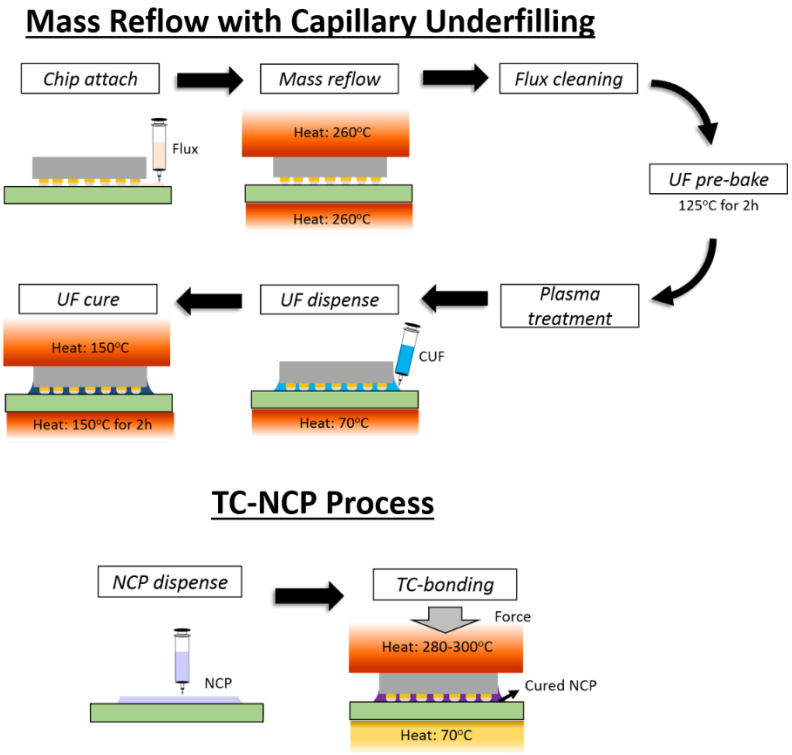


Figure 12. Process flows of mass reflow with capillary underfilling (CUF) and TC-NCP.

Despite such outstanding benefits, TC-NCP has achieved only limited adoption in high-volume manufacturing (HVM). Application of pressure during assembly requires more complex and expensive equipment and a complete change in infrastructures,

investment that only major OSATs like Amkor can afford. Unlike mass reflow, TC-NCP is not a batch process, giving a much lower throughput of typically <1000 units per hour (UPH), two orders of magnitude, at least, less than in conventional reflow. Throughput of thermocompression bonding is essentially defined by the time required for NCP dispensing and assembly of individual dies, estimated to about 7s today. This cycle time is primarily controlled by the thermal budget required to melt the solder, as well as heating and cooling rates applied on die side. Because NCP is dispensed on substrate, the stage temperature cannot be increased above 90°C, forcing to rise the chip temperature to about 300°C to reach the melting point of solders.

Some studies has been conducted to address those limitations in R&D, either from the underfill material side or assembly infrastructure. The Wafer-level non-conductive films (WL-NCF) that can be directly laminated on bumped wafers before dicing were developed. This approach eliminates the need for underfill dispensing and constraints on stage temperature, as well as enables more accurate underfill volume control. Amkor recently claimed that TC-NCF combined to a gang-bonding strategy can compete with the cost of mass reflow in cost if at least 8 dies are simultaneously bonded [93]. Additionally, advances in tools towards higher heating and cooling rates have concurrently brought significant improvements in UPHs. Kulicke and Soffa recently launched their APAMA bonder series capable of heating and cooling at up to 400 K/s, demonstrating TC-NCF assembly with 1500 UPH closing the cost gap with reflow [94]. However, the NCF technology is still young and faces several challenges hindering its large-scale adoption: (a) voiding introduced by film lamination; (b) delamination and material degradation in dicing; (c) higher bonding forces than with NCPs; (d) post-assembly voiding due to poor

adhesion and over curing, particularly on organic substrates [95, 96]. In addition, the laser-assisted bonding (TAB) in replace of direct heating of TC-bonding was recently introduced by Amkor to maximize the throughput. A specialized near infrared laser was implemented to heat the die with high directionality, uniformity and selectivity. It has been confirmed that the bonding time could be shorten to 1-2s, while all the benefits granted from localized heating is kept [88]. Another potential technology is the ultrasonic or ultrasonic-assisted bonding, which could be directly implemented on current thermocompression bonder. The technology has been demonstrated to improve the throughput by accelerating the intermetallics formation and to enable the soldering under ambient temperature. With the same bonding time of 10s, a 10µm-thick Cu-Sn SLID joint can completely transform with the assistance of 35 kHz ultrasonic frequency, benchmarking a ~1µm Cu-Sn intermetallic if using TC-bonding only [97]. However, those technologies were still questionable for their scalability and far from being adapted by HVM.

CHAPTER 3. TEST VEHICLE AND DESIGN OF ASSEMBLY PROCESS

This chapter describes the test vehicle fabrication and assembly process, categorized into two sections. The section 3.1 describes the design and process flow of the substrate and die used in this thesis, scaled from the pitch size of 100µm, 50µm down to 20µm. The section 3.2 focuses on the design of TC-NCP process, followed by the experimental justification. The basic understandings from section 3.2 enabled the assemblies through this thesis.

3.1 Test vehicle design and fabrication

3.1.1 Test vehicle 1 (TV1) at 100µm pitch

The TV1 was used for EPAG surface study with Sn2.0Ag 10µm /Cu 15µm microbumps. This test vehicle contains 760 I/Os with daisy chain test structure, including peripheral rows at 100µm pitch and central array at 250µm pitch, as showed in Fig. 13.

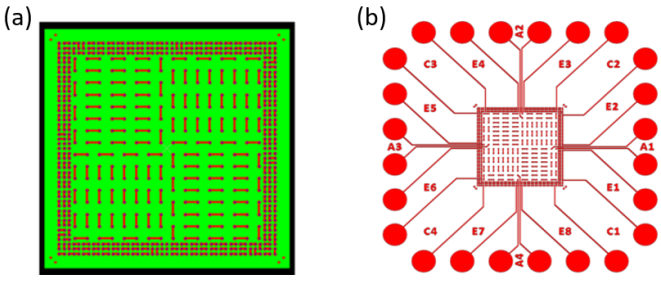


Figure 13. The TV1 design of (a) die, and (b) substrate

For the substrates, a subtractive process was used with the copper clad 1mm-thick FR-4 boards. First, the 35µm-thick copper clad was thinned down to 7-10µm through Cu

etchant of $CuCl_2$ and HCl. To optimize the etched copper surface and enhance the uniformity, a microetching process with Securiganthetch Cleaner C chemical from Atotech was followed for 10mins. The Cu clad was then patterned with negative-toned dry film photoresist Hitachi-RY5315EB. The unexposed regions were then removed by same Cu etchant chemical. The fabricated substrates were applied the EP, EPAG, and ENEPIG surface finishes. Chemistry Pallabond Pd was for EP, Pallabond Pd/Au for EPAG, and Aurotech CNN/PD Tech PC/Aurotech SF Plus for ENEPIG. Fig. 14(a) and (b) shows the substrate process flow and the fabricated substrate before surface finishing, respectively.

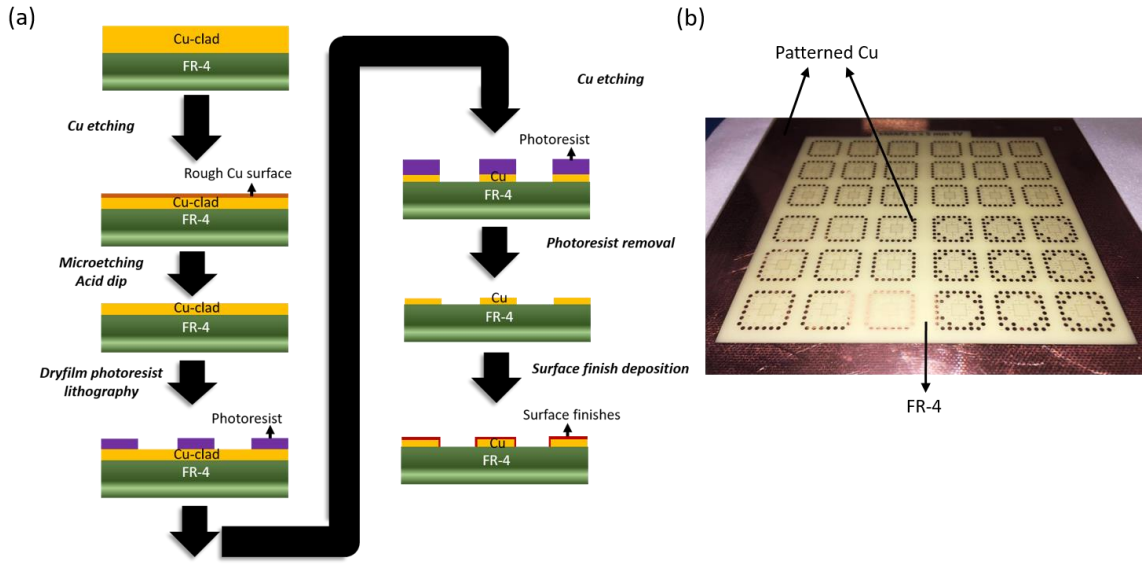


Figure 14. (a) The process flow, and the (b) fabricated FR-4 substrate of TV1

The dies were fabricated with a 600µm-thick silicon wafer. A thermally-grown SiOx was fabricated with Lindberg Furnace as the dielectric, and a sputtered Ti/Cu layer was then deposited as the seed and adhesion layer with CVC DC Sputterer. A two-step additive process was applied for the copper routing and the bump with the photoresists of Hitachi RY-5315UTB and Hitachi Sample A. A Karl Suss TSA MA-6 Mask Aligner was

used for aligning the bump to the routing with 0.2 micron top alignment resolution. After each photoresist developing step, the resist residuals were cleaned through the descum with Plasma Therm RIE. A SolderFill-Ag800 chemical was used for SnAg electrolytic plating, and the plated composition was found related to the plating current density. In this study, a composition of Sn2.0Ag was achieved, corresponding to a plating rate of 1.5 ASD. After bumping, the Ti/Cu seed layer was etched by the Copper Etch 49-1 from Transene Company Inc. and HF. Fig. 15(a) shows the fabricated microbumps of 10µm-thick Sn2.0Ag and 10µm-thick Cu. A total variation of 0.6µm was measured with 10 bumps within one die, and 5 dies through a 6" wafer on the Olympus LEXT 3D Material Confocal Microscope, as showed in Fig. 15(b).

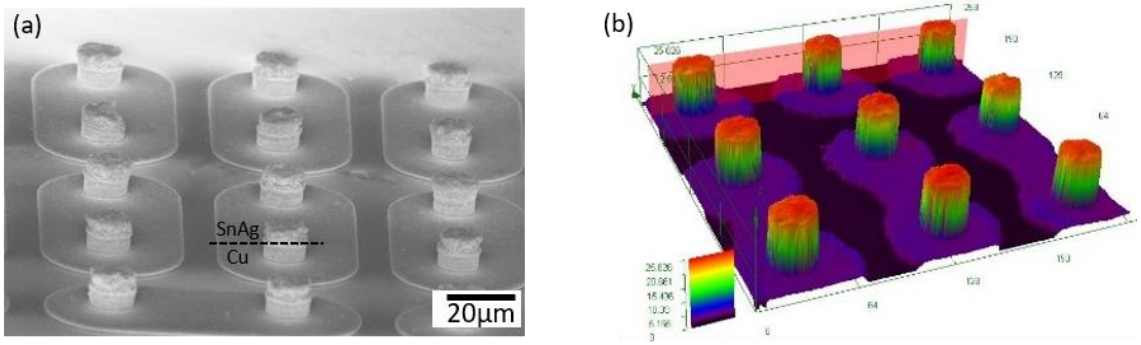


Figure 15. The (a) tilted SEM image, and (b) confocal measurement of the fabricated Cu microbumps.

3.1.2 Test vehicle 2 (TV2) at 50µm pitch

The TV2 was designed with a bond-on-trace (BoT) structure and composed of a single peripheral daisy chain at 50µm pitch. Fig. 16 shows the design of TV2, which contains 544 I/Os. Two different core materials were used in this study, one is a 200µm-thick Hitachi E679FG-S organic material and another is a 100µm-thick low-CTE glass

from Asahi Glass Corporation. The organic substrates stripe were supported by Walts Corporation, as showed in Fig. 17(a), and then singulated in GT-PRC with the DISCO Automatic Dicing Saw DAD3360. Fig. 17(b) shows the build-up structure of those organic substrates, which contains two dummy mesh layers and two Cu routing layers. An industry standard ABF-GX series build-up material and solder resist were applied. The organic TV2 substrate will be bonded with standard Cu microbumps, composed of 15µm Sn3.5Ag/2µm Ni/30µm Cu, as the platform of designing the TC-NCP process and also studying the EPAG surface finish. The cross-section of standard Cu microbump from Walts Corporation is showed in Fig. 17(c).

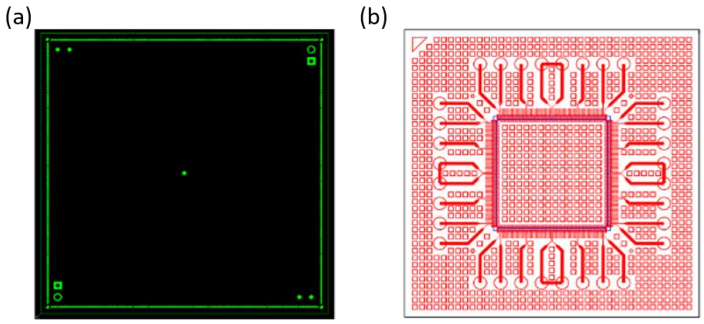


Figure 16. The TV2 design of (a) die, and (b) substrate

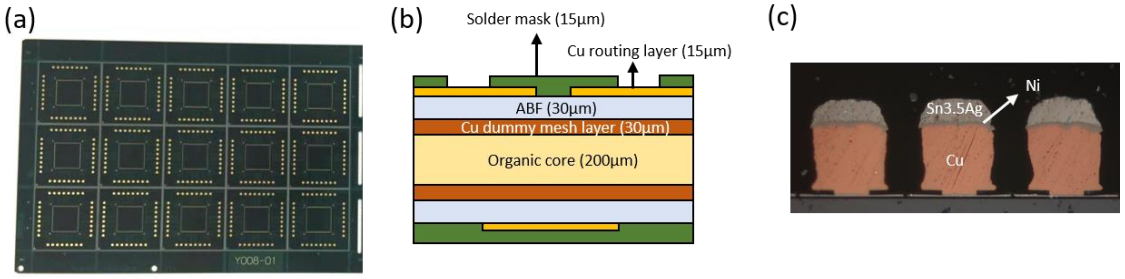


Figure 17. (a) Top view, and (b) build-up structure of organic substrate; (c) the standard Cu microbump, supported by Walts Corporation.

GT-PRC has been dedicated for years to developing ultra-thin glass interposers for next generation high performance electronics, driven by the potentials of high-density routings with reduced electrical loss, tailorable mechanical properties, and panel-level process at low cost. As part of this activity, 100μm-thick glass substrate with TV2 design was co-developed in house with the technical support of NGK Spark Plug Corporation. First, an O_2 plasma and silane treatment were applied on bare glass to enhance the adhesion of build-up laminate. An ABF-GX92 film from Aginomoto Corporation was vacuum laminated with Hi-Vac-600 Drawer Vacuum Laminator, and then secured with hot pressing. The seed layer was then formed on the ABF film with a Printoganth MT electroless Cu chemical. The similar additive process was used to form the Cu routings, including the lithography and Cu electrolytic plating as described in TV1. Since Pd was normally used as the catalyst of electroless Cu process. After the Cu seed layer removal, a Finelise-JCU chemical was applied to eradicate the Pd atoms adhering to the ABF in case of Pd contamination. Before applying the Hitachi SR-FA solder resist, a BondFilm process from Atotech was introduced for improved adhesion. In the end, an ENEPIG surface finish was deposited. The process flow and the fabricated glass substrate after singulation are showed in Fig. 18.

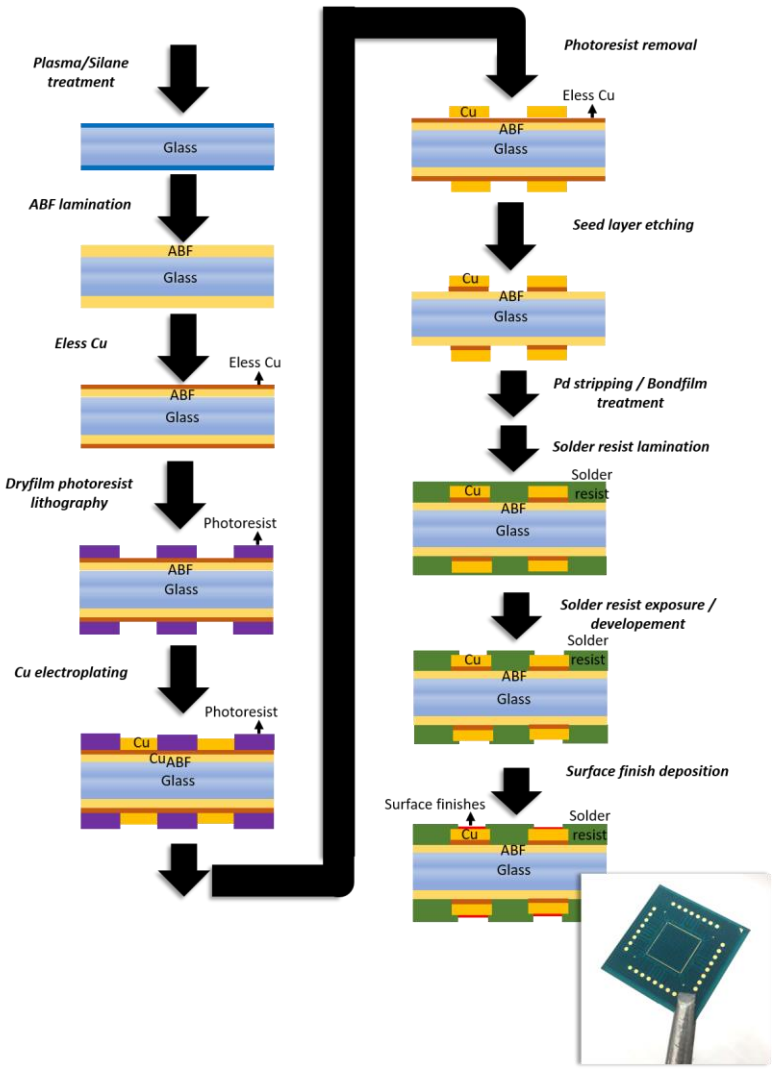


Figure 18. The process flow of glass subtrate of TV2

3.1.3 Test vehicle 3 (TV3) at 20µm pitch

To demonstrate the off-chip interconnections below 35µm pitch, a new test vehicle was designed with single peripheral row at 20µm pitch, and 860 I/Os. Fig. 19 shows the design of TV3. A short daisy chain circuit at each edge was designed for testing only four joints through electromigration reliability test. A Si substrate was used as the first demonstration, enabled by the process flow described in Fig. 20(a).

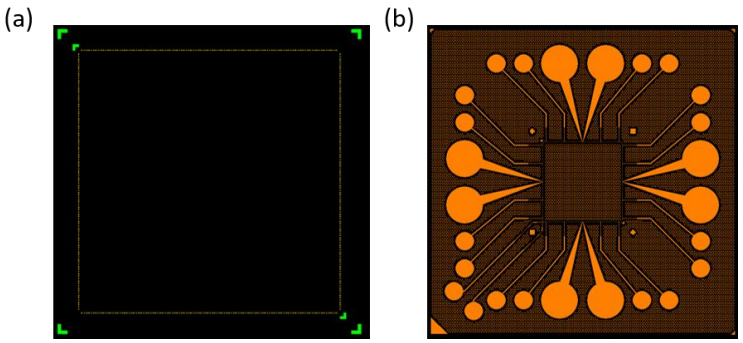


Figure 19. The TV3 design of (a) die, and (b) substrate.

A TMMR-PW1000T-PM photoresist from TOK Corporation was spin coated on a 4-inch wafer with SiOx dielectric and sputtered Ti/Cu seed layer. The maximum spinning speed was reduced to 3000 rpm for a film thickness of 2-3μm. After exposure with a dose of 180 mJ/cm^2, TMAH (Tetramethylammonium hydroxide) was used for development. An O_2 plasma with Plasma Therm RIE was used for descum. The uniformity of electroplated Cu was achieved by the dummy feature populated through the substrate and the reduced plating rate of 0.75 ASD. A ST-121A resist stripper from TOK Corporation was then used for dissolving the photoresist. A Copper Etch 49-1 chemical from Transene Company was used for etching the sputtered Cu layer. And the underneath Ti was etched by the plasma with the mixtured gas of 45sccm CHF_3 and 5sccm O_2. After the ENIG surface finish deposition, no extraneous plating of ENIG surface finish was observed within 10μm feature gap, as showed in Fig. 20(b).

Being constrained by the interconnections design rule for 20μm pitch, a bump with 7μm in diameter and 10μm in height is required on the die. An intensive optimization of lithography condition was conducted to scaling down the spatial limitation of dry film photoresist, Hitachi 5315-UTB. As showed in Fig. 21(a), the concern of distorted or

missing bumps was found with the suggested exposure condition of 150 mJ/cm^2, possibly caused by the material expansion of negative-toned photoresist during crosslinking. To compensating this dimensional deviation, an under exposure condition of 130 mJ/cm^2 was then selected to achieve well-developed bump openings. Fig. 21(b) shows the electroplated bumps with a 7μm diameter, yielded with the optimal condition.

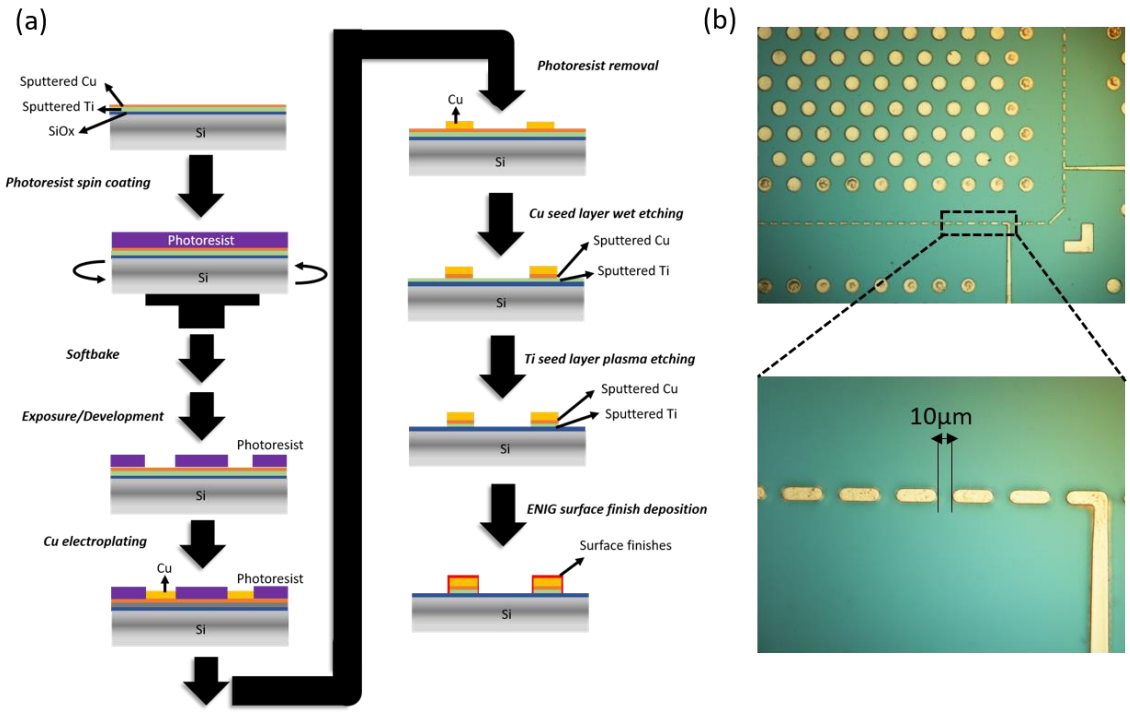


Figure 20. The (a) process flow, and (b) fabricated Si substrate of TV3.

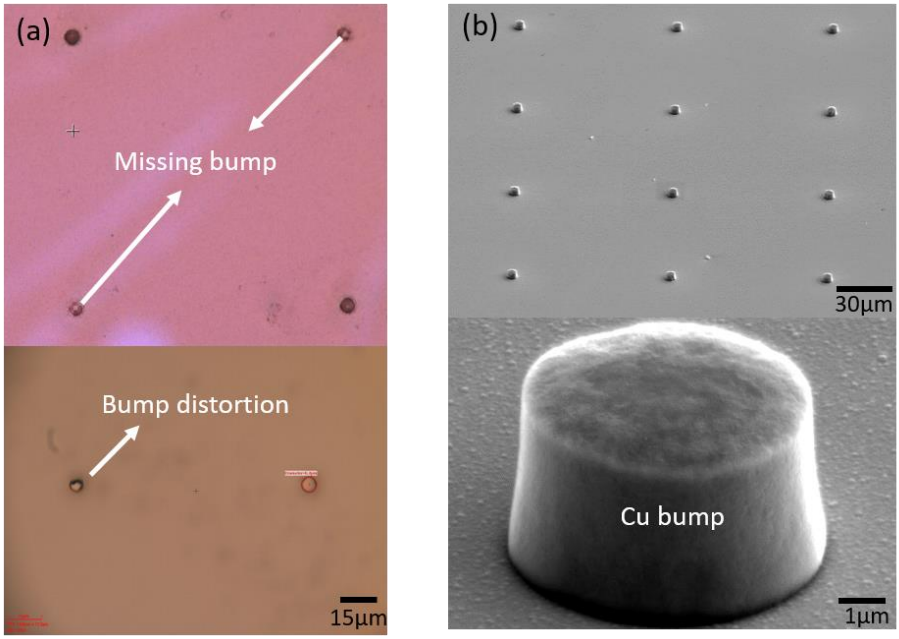


Figure 21. The 7µm Cu bump (a) before, and (b) after lithography optimization.

3.2 Design of thermocompression bonding with nonconductive paste (TC-NCP)

This section aims at understanding the basics of thermocompression bonding (TC-bonding) with pre-applied underfill, considering interactions between processes, materials, bonder and package design to provide guidelines for process design in production conditions, without the need for empirical trials and error routine. In particular the thermal profiles have to account for heat transfer through the package, which is conditioned by the substrate design. To illustrate this point, the average thermal conductivities measured by laser flash method of substrates with varying core material, thickness, number of metal routing layers and densities of through-package vias (TPVs) are listed in Table. 6. Given these results, it is clear that the TC-bonding conditions have to be customized according to the package design for controlled interfacial reactions and intermetallics formation. In

particular, ultra-thin glass substrates, pioneered by Georgia Tech PRC as the next frontier for system scaling and considered in this work, are still in development and have consequently not yet been qualified in production environment. In this section, a FEM model of a fully-integrated glass package with realistic electrical design was first built to accurately capture its thermal behavior. A coupled-field model emulating a real-time TC-NCP process was then solved stepwise. Assembly trials have finally been carried out to verify the accuracy of the FEM models' predictions.

Table 6. The average thermal conductivities of different substrates, measured by laser flash method. (Courtesy of Namics Corporation)

	TV1	TV1	TV1	TV1	TV2 with TPV	TV2 no TPV
Core Material	Organic	Organic	Organic	Glass	Glass	Glass
Core thickness (μm)	200	200	100	100	100	100
Metal layers	4	2	2	2	4	4
Specific heat (J/g.K)	0.5036	0.7461	0.7198	0.6351	0.5619	0.6149
Density (g/cm^3)	2.4757	1.9909	2.1575	2.3620	2.4787	2.5365
Average thermal conductivity (W/m.K)	0.3625	0.2373	0.4540	0.5590	0.5090	0.5550

Metal layer effect *Thickness effect* *Core material effect* *Via effect*

3.2.1 Full package thermal modeling

To simulate the thermal behavior of a fully-integrated glass package, a finite element model was built in accordance with the electrical design of Fig. 22 emulating a single-chip application processor (AP) package. The package is composed of a low-CTE glass substrate laminated with ZIF-ZS-100 polymer dielectric build-up layers from Zeon Corporation supporting 4 routing layers numbered M1-4 from chip to board side. Through-

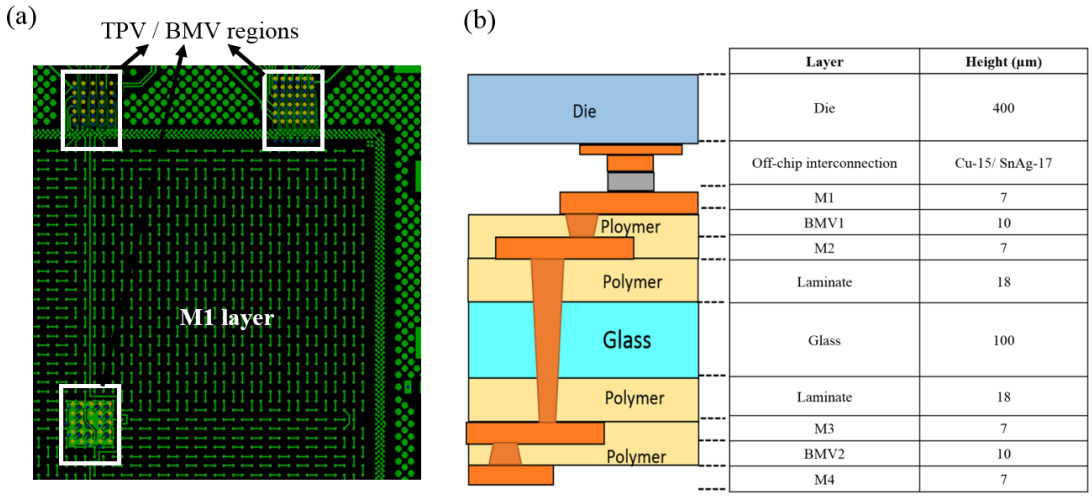
package vias (TPVs) at 170µm pitch connect the M2 and M3 layers through the glass, and blind micro-vias (BMVs) at 120µm pitch interconnect the stacked metal layers M1 and M2, and M3 and M4, respectively. On die side, the interconnection system is constituted of a 3µm-thick Cu pad, a Cu pillar micro-bump, 15µm in height and 26µm in diameter with a 17µm Sn3.5Ag solder cap, at 80µm pitch, and a development NCP material from Namics Corporation. The material properties applied in the models are summarized in Table 7.

Considering the difficulty of capturing this complex design in a single model, equivalent thermal models of individual off-chip interconnection with NCP, BMV and TPV were first established to estimate the equivalent thermal conductivity of these structures. Both realistic models, whose geometry was directly based on the electrical design, and equivalent models were built in ANSYS as detailed in Fig. 23. The represented geometries were defined by the interconnection, BMV and TPV pitches. Heat flow boundary conditions cannot be directly applied on the modeled structures as it would not provide an accurate representation of the heat distribution in the structure due to large discrepancies in material properties. Pseudo-perfect thermal conductors with a conductivity of 10^6 W/m.K were consequently introduced at the top and bottom of all geometries to spread the heat and improve the accuracy of the loading conditions. A temperature of 25°C was then applied at the bottom of all geometries while a heat source of 0.1W was applied on their top surface. In-plane thermal conductivities were assumed to be the same as that of the matrix materials. The equivalent Z-direction thermal conductivities were finally determined by matching the top surface temperature results from the realistic model under these boundary conditions. The equivalent conductivities of

an interconnection, BMV and TPV were of 3, 34.5 and 1.8 W/m.K, respectively. These equivalent thermal conductivities were then input as material properties in the thermal model of the full package.

To model the thermal behavior of the fully-integrated package in TC bonding, the boundary conditions need to account for interactions with the environment and the bonding tool. Therefore, the air convection coefficient, thermal interface conductance between the tool head and the top of the die, as well as between the heating stage and the bottom of the substrate have to be determined. The latter are tool-dependent and were qualified for the lab-scale Finetech Matrix semi-automatic bonder at this time. FEM models were constructed to emulate the thermal experiments of Fig. 24(a), (b) so as to determine these parameters. In the first experiment, a thermal interface material (TIM) with known thermal conductance of 25 W/K was applied between a FR-4 substrate and the bonder stage as shown in Fig. 24(c). Thermocouples were used to measure the temperature of the top surface of the substrate in multiple locations with varied stage temperatures. The only unknown in this experiment is the air convection coefficient, which can be determined through modeling by matching the measured temperature map. This parameter was evaluated at 55×10^{-6} W/mm^2.K, slightly exceeding reported valued for natural air convection, ranging from 10 to 20×10^{-6} W/mm^2.K, which is to be expected in a lab environment with forced air circulation. The second experiment aims at evaluating the heat transfer coefficient of the thermal interfaces with the tool head and stage of the bonder, as shown in Fig. 24(d). The coefficients of both interfaces was assumed identical as a first approximation. In this experiment, a FR-4 substrate was sandwiched between the tool head and the stage. Thermal gradients of different magnitudes were then applied by varying the

tool head temperature. The temperature of the top surface of the substrate was again measured in different locations and correlated to modeling predictions to extract the heat transfer coefficient of the contact interface. The latter was determined to be $5x10^{-4}$ $W/mm^2.K$.



Layer	Height (µm)
Die	400
Off-chip interconnection	Cu-15/ SnAg-17
M1	7
BMV1	10
M2	7
Laminate	18
Glass	100
Laminate	18
M3	7
BMV2	10
M4	7

Figure 22. . (a) Electrical design of fully-integrated application processor glass package and (b) detailed cross-section view of package stack-up.

Table 7. Material properties implemented in FEM modeling.

Isotropic mechanical properties

Materials	Silicon	Glass	ZIF (ZS-100, Zeon)	NCP (Namics)	Cu_6Sn_5
E(GPa)	129.85	72	7.7	6.5	52.4
Poisson's ratio	0.28	0.23	0.132	0.4	0.34
CTE (ppm/K)	2.56	6	25	33	21.85
$T_{ref.}$ (°C)	230	160	160	175	230

Bilinear kinematic hardening model for copper

Parameters	Value
E(GPa)	103
Poisson's ratio	0.3
CTE (ppm/K)	17.0
Initial yield stress (MPa)	172.38
Tangent modulus (MPa)	1034.2
Tref. (°C)	110

Anand's viscoplastic model for Sn3.5Ag

Parameters	Value	Parameters	Value
So (MPa)	39.09	H_0 (MPa)	3521.5
Q/R (K)	8900	M	0.13
A	22300	n	0.018
X_i	6	a	1.82
S_h (MPa)	73.81		

Isotropic thermal properties

Materials	Thermal conductivity (w/m.k)	Specific heat capacity (J/kg.k)	Density (g/cm^3)
Silicon	149	730	2.33
Copper	401	379	8.94
Sn3.5Ag	55	234	7.40
Glass	1.3	840	2.50
ZIF	0.52	920	1.15
NCP	0.3	1130	1.4

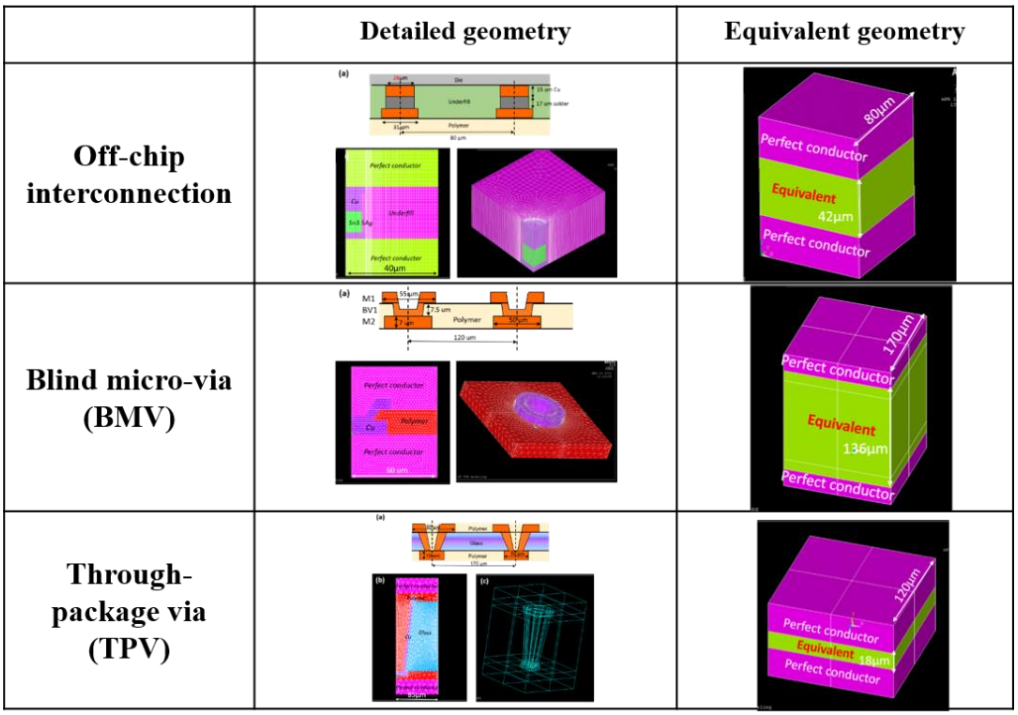


Figure 23. Detailed geometries and corresponding equivalent models for off-chip interconnection, BMV and TPV.

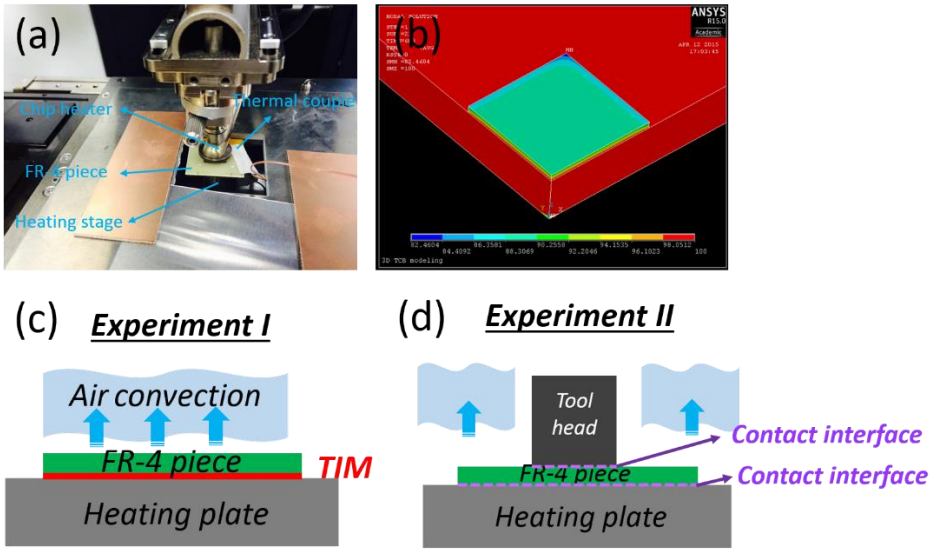


Figure 24. Thermal model calibration with a) experimental setup and (b) corresponding FEM model, to determine (c) air convection coefficient, and (d) thermal contact conductance.

Previous models and experiments enabled the determination of all material properties and boundary conditions required to model TC-NCP assembly of a fully-integrated glass package, as shown in Fig 25. Thermal profiles applied in actual TC-NCP process were implemented as boundary conditions of this new model. The stage temperature was consequently maintained at 70°C while the tool head temperature was ramped to a variable peak temperature. Temperatures at the top of the die, bottom of substrate and in the solder were extracted and plotted in Fig. 26 and Fig. 27 as a function of the tool head peak temperature for a glass package with two (M1 and M4 only) and four metal layers, respectively. As the considered glass package is very thin, with a core thickness of only 100µm, it is difficult to build a significant thermal gradient across it. A tool head peak temperature of 400°C was, therefore, required to melt the solder in the 2-metal-layer package. The average thermal conductivity of the substrate is expected to increase with the number of metal layers as indicated by the results of Table 6. The temperature achievable in the solder in the same bonding conditions subsequently dropped to 178°C in a 4-metal-layer package. As 400°C is the maximum tool head peak temperature applicable by most production TC bonders, it would not be possible to assemble this test vehicle without increasing the stage temperature. The current trend to ultra-thin high-density substrates thus brings new challenges for TC-bonding which can only be solved by breakthrough advances in tools and wafer-applied underfill materials. In addition, the substantial drop in temperature by 30-50°C observed in the solder between the two evaluated package configurations illustrates the strong dependence of the TC bonding conditions on the package electrical design and need for highly-customized process recipes. This large temperature discrepancy can be further explained by considering the

flux vector plots. A significant lateral heat flux was found in the metal layers, dissipating the heat from the center to the periphery of the 4-metal-layer package. Such lateral heat flux was inexistent in the 2-metal-layer package.

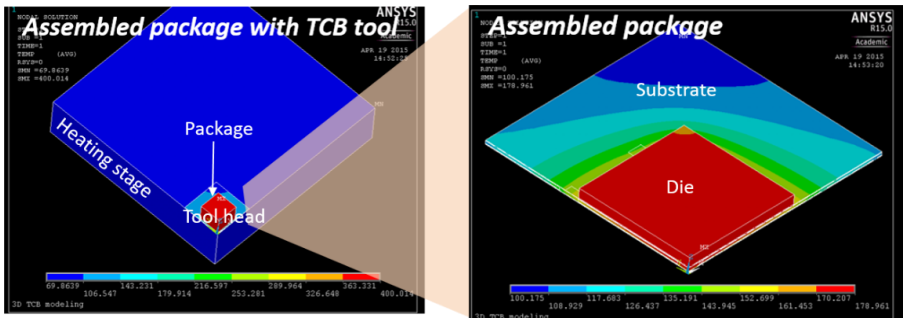


Figure 25. Fully-integrated glass package FEM modeling

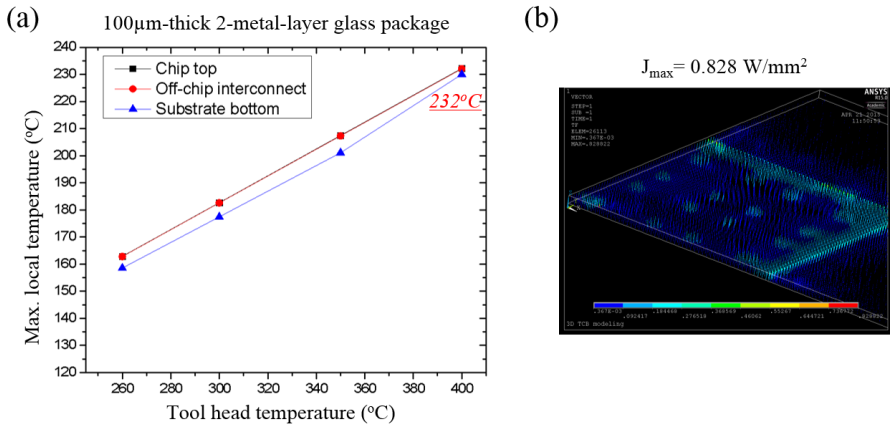


Figure 26. Thermal modeling of assembly on 2-metal-layer glass package with (a) temperature distribution vs. tool head peak temperature, and (b) heat flux vector plot.

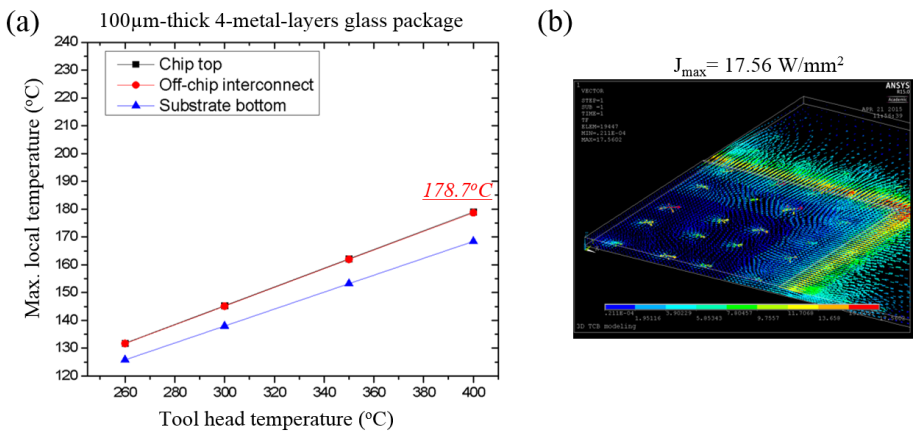


Figure 27. Thermal modeling of assembly on 4-metal-layer glass package with (a) temperature distribution vs. tool head peak temperature, and (b) heat flux vector plot.

Except of the effects of the packaging architecture, the thermal interaction between flip-chip bonder and package could also be studied through repeating the procedure described in Fig. 24 with different classes of tool. In GT-PRC Interconnection and Assembly laboratory, a lab-scale flip-chip bonder from FINETECH and a full automatic APAMA Chip-to-Substrate Thermo-Compression Bonder from Kulicke & Soffa Corporation were used for comparison. As showed in Fig. 28, an improvement of heat transfer coefficient on the thermal interface of bonding heat and die was found by around three-orders of magnitude. With the heat transfer coefficient of 5×10^{-4} W/mm^2.K, the achievable off-chip interconnection temperature is 178℃, while applying a 400℃ tool head temperature on a 100µm-thick 4-metal-layer package. In comparison, the standard reflow temperature of 260℃ can be easily reached with a lower tool head temperature of 290℃, with the heat transfer coefficient of 10^{-1} W/mm^2.K.

This significantly different thermal behavior between tools have aggravated the throughput limitation of lab-scale tool, since an extended heat cycling time is required for

a higher peak bond head temperature. In addition, such difference could also be found on the transient thermal behavior. The insufficient heat transfer on the interface corresponds a limited temperature ramp rate at off-chip interconnect. An example was taken with the transient thermal model that stimulates the condition of a 100μm-thick 4-metal-layer package, assembled with a nominal ramp rate of 6K/s and 200K/s. The actual temperature of off-chip interconnect is plotted in time domain in Fig. 29. While the curves of 200K/s ramp rate were used as the benchmark that can achieve the steady temperature within 4s, a dwell time of 60-65s is required before reaching the peak temperature with a 6K/s ramp rate.

Such low temperature ramp rate indeed conflicts to the curing kinetic of pre-applied underfill materials, since the most of pre-applied underfill materials, such as snap-curing NCP, was developed for high temperature ramp rate with the interest of high throughput. With low heat transfer coefficient and temperature ramp rate, the NCP would be over-cured before reaching the target reflow temperature, and cause serious concerns of non-wetting or silica filler entrapment. Furthermore, according to the temperature distribution captured in Fig. 27, a localized high temperature was found at the bottom of the substrate, right beneath the bonding area. With such complex temperature distribution, it becomes difficult to predict the warpage behavior in TC bonding. Arising for this research, a new project was initiated in collaboration with Kulicke and Soffa to fundamentally understand TC-induced warpage with varying thermal and force profiles, in production conditions. This project aims at providing guidelines for optimization of assembly conditions for minimum warpage.

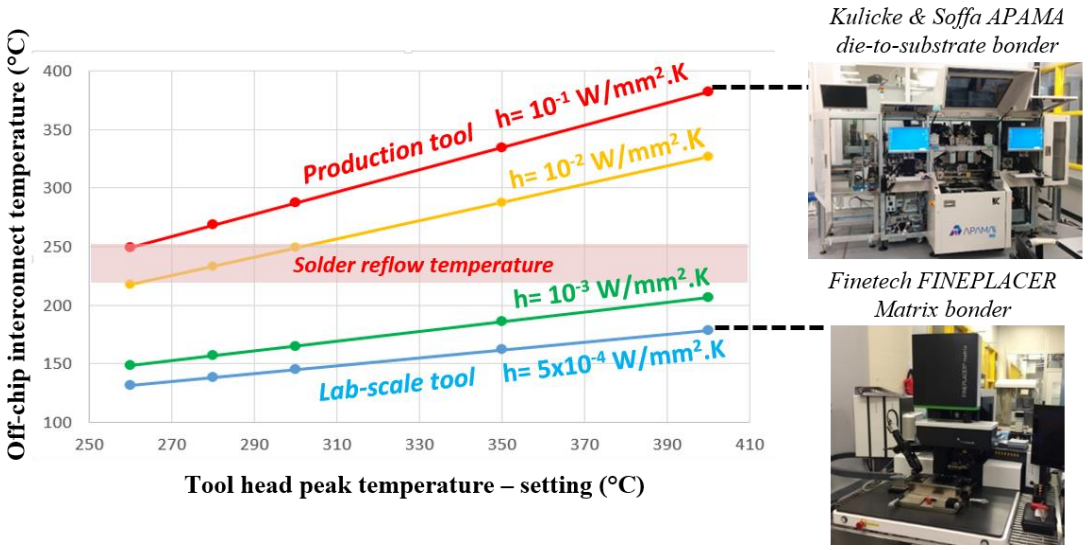


Figure 28. The off-chip interconnect temperature vs. tool head peak temperature with varied heat transfer coefficients of thermal interface.

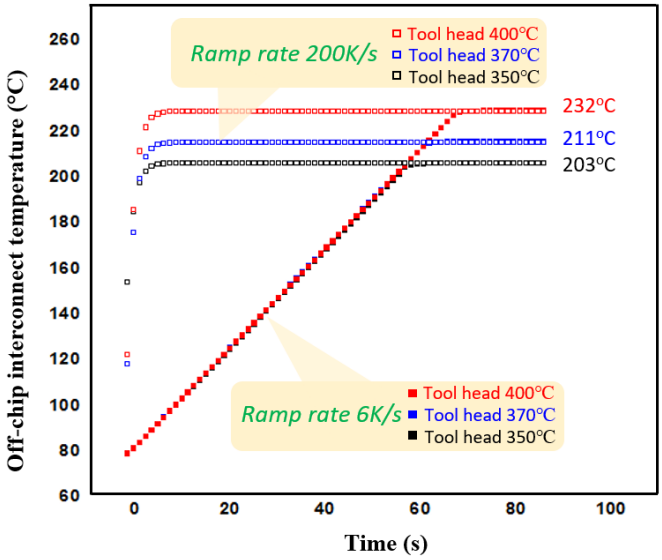


Figure 29. The off-chip interconnect temperature evolution in a transient thermal modeling with ramp rate of 200K/s and 6K/s.

3.2.2 Coupled field processing modeling

As mentioned in Section 3.2.1, the ideal TC-NCP model needs to consider the actual temperature distribution, the interaction of bonding profile and material, and also

the transient evolution through the process. Therefore, a multiphysics process model was set to clarify the dynamics interaction between temperature, pressure and materials through the assembly, ultimately providing the guidelines of optimizing the thermocompression bonding condition.

The general TC-NCP process recipe and corresponding evolution at each time step is described in Fig. 30. The NCP is first dispensed on the bonding area with accurate volume control. An increased pressure is then applied when reaching NCP's low viscosity point (t1), to enable the ideal contact between solder bump and Cu pads. With the increasing temperature, the NCP is projected to be partially-cured at its gelation point (t2) around the melt point of solder. This t2 sat within a small process window has been considered as the key of controlling the solder collapse and subsequent bonded reliability. Since the gelled NCP could contribute to the strength of bonding and confine the molten solder after t2, the evolution of high interest can be expected to happen mainly within the timeframe between t1 and t2. Therefore, the model's geometry was setup of assuming the solder bump to be landed on the Cu pads at the beginning, and the model ended when the temperature reached the gelation point of NCP material.

However, the main blind spot in manufacturing is the deviation of actual temperature distribution from the nominal temperature set in the recipe, as the dark red curves printed in Fig. 30. In addition, the NCP's gelation point (t2) could shift under different temperature ramp rates. In this modeling, the actual temperature distribution could be perfectly addressed by applying the outputs of aforementioned full-package thermal model as the temperature boundary condition. The behavior of NCP's gelation point was

simulated by adjusting the time step between t1 and t2, defining by the actual temperature and the temperature ramp rate.

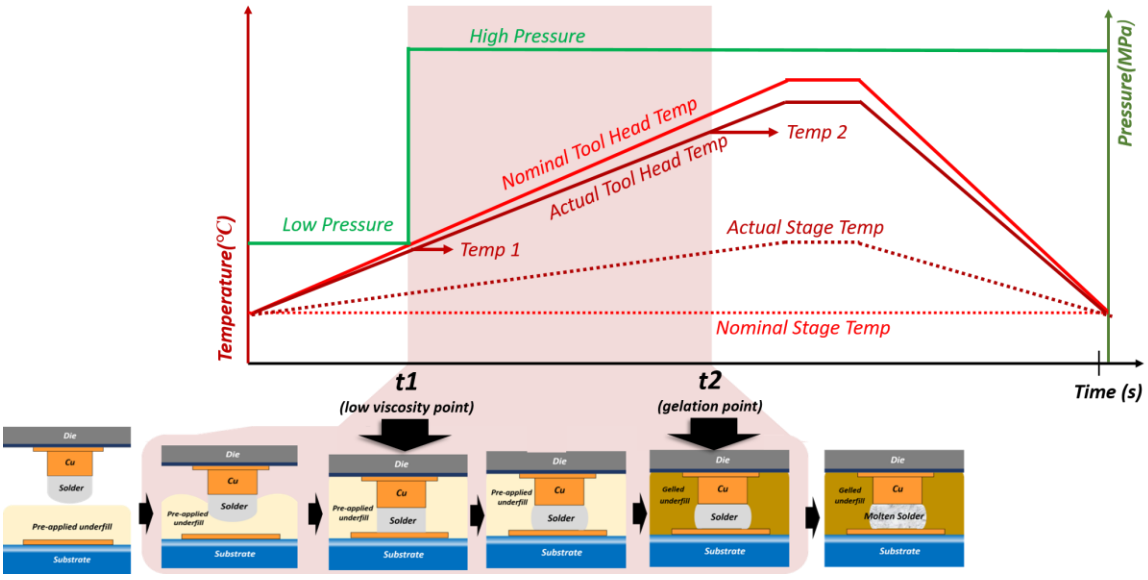


Figure 30. The evolution of TC-NCP process through the bonding profile.

An 8-node coupled field plane 223 element was used in the multiphysic modeling under axisymmetric condition. The solder height was initially set as 15μm with a 30μm diameter. The X-displacements of all the nodes located on the symmetric boundary were set as zero, and the Y-displacements along the bottom of the whole structure was constrained as zero. In addition, since the repetition of the same structure, the X-displacements of all the nodes located at the right boundary were coupled, sharing the same value. The material properties listed in Table 7 was applied, and a Young's Modulus of 0.1GPa was assumed for the non-cured NCP material.

The low pressure of 2MPa and the high pressure of 40MPa were initially defined by the instructions of NCP and was loaded on the top surface of die in this modeling. For

temperature profile, the real temperature collected from thermal modeling at different timings were applied on the top surface of die and the bottom of interposer, building the approximate temperature gradient to the real case. Two cases were used for preliminary demonstration, as showed in Fig. 31 and Fig. 32. The Fig. 31 mimicked the lab-scale flip-chip bonder, having a gelation point of 170℃ with a 6K/s ramp rate. Between t0 and t1, a solder collapse of 0.2μm is negligible due to lower pressure and temperature. The solder height was found reduced to 11.4μm while a large pressure of 40MPa was applied at t1. During the period with high pressure, the solder height was further shorten from 11.4μm to 9.5μm. This result reflects the scenario that the NCP is cured at a lower temperature and provides solid solder confinement. In Fig. 32, the conditions of a production flip-chip bonder was applied, having a gelation point of 230℃ corresponding to a 100K/s ramp rate. A significantly reduced solder height of 4.9μm was modeled at t2, caused by the elevated temperature than the case of Fig. 31. This model indicates a failed solder collapse control due to the insufficient solder confinement of NCP.

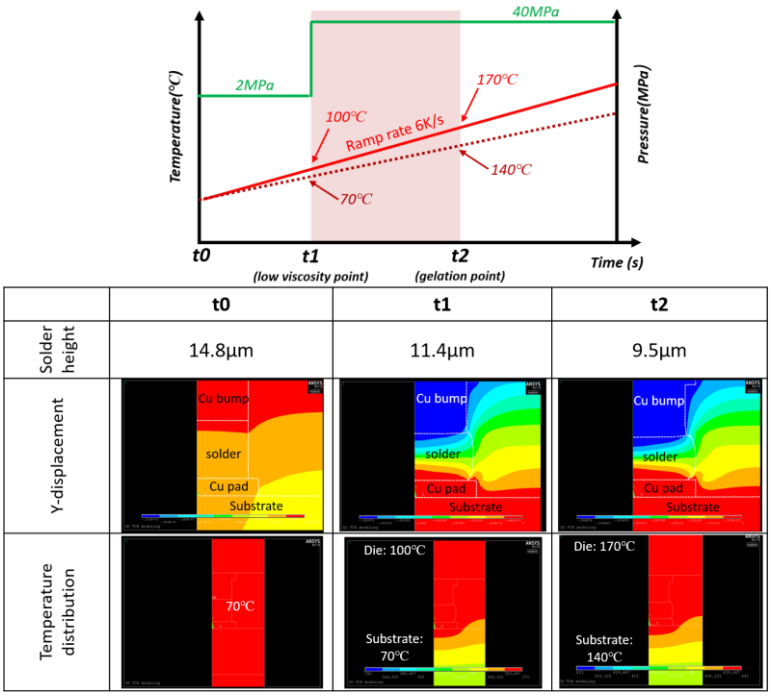


Figure 31. The plots of Y-displacement and temperature distribution under the condition of lab-scale flip-chip bonder.

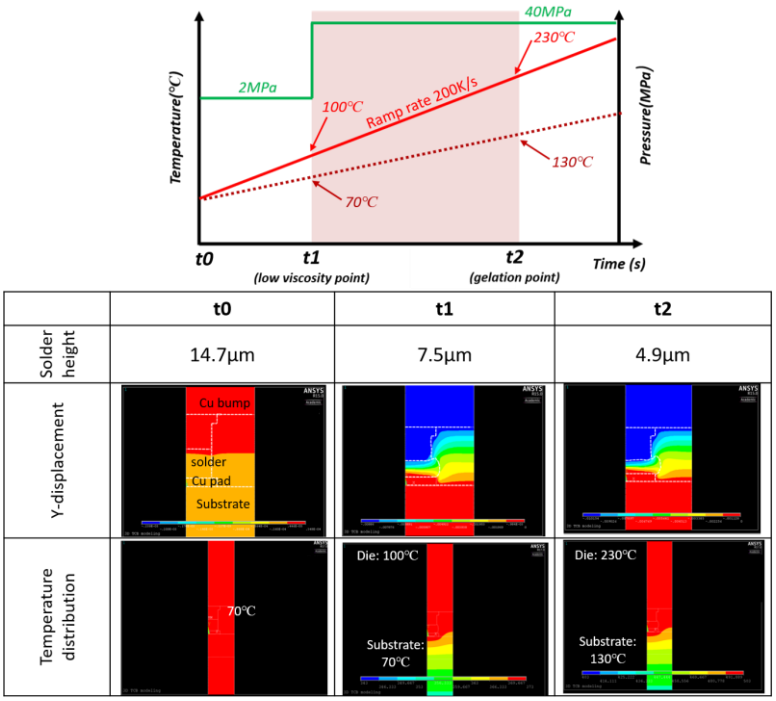


Figure 32. The plots of Y-displacement and temperature distribution under the condition of production flip-chip bonder.

In this section, a systematic methodology of designing TC-NCP process was established without tedious trial-and-error process optimization. At first, the actual temperature distribution through package was accurately predicted through thermal modeling. And then the real-time actual temperature distribution, pressure and NCP material evolution could be imported into the multiphysics modeling, used for predicting the as-bonded solder joints. However, several technical challenges are still remaining and beyond the capability of accessible resources:

1. The NCP material property in current model is highly simplified by assuming as an extremely soft material. Even it's believed that the non-cured NCP material would not contribute significant mechanical strength, the real NCP material property also has a transient behavior. But normally, only the fully-cured NCP's mechanical properties will be measured and reported. To fully capture the penetration of bump through non-cured NCP, some rheological measurements of non-cured NCP need to be conducted and fitted with appropriate non-Newtonian fluid models. However, a multiphysic transient element including mechanical, thermal and fluidic flow is not available.
2. In current modeling, an Anand's viscoplastic model was referenced for SnAg solder. However, even the factor of varied temperature is considered in the formulation by fitting the material parameter (c) and internal variable (s) as functions of temperature, the temperature range is mostly limited to that lower than $0.65T_m$. The behavior of solder increasingly deviates from reality when the temperature approaches the melt point of solder. Some

mechanical properties of common solder at elevated temperature are available, but the special time-factor gained with viscoplastic model will miss if using those measured properties as an elastic material.

3. In the preliminary model, all the areas including that for NCP are glued. However, since a glide on the solder, Cu/NCP interface is expected, an improved description of those interfaces is required. A modification of the initial process model was conducted with the concept of contact element. The elements of Conta 172 and Targe 169 were applied and overlaid on theses boundaries, and the contact behavior was assumed to be bonded at beginning. The standard contact stiffness was set as default, and the allow penetration and frication were set as 0 for preliminary approximation. As showed in Fig. 33, a risk of underfill delamination was implied by the model with a severe solder deformation caused by a 40MPa pressure. And a gap between solder and landing pad was found, which could allow the underfill material flowing back beneath the solder joints. The concept of using contact element seems promising to improve the process model, but an in-depth understanding of the interface with NCP is required.
4. A highly distorted element was commonly found through the process modeling, due to the solder's and NCP's soft material properties and the high bonding pressure. This challenge is constrained by the fundamental limitation of FEA. The new concept of adaptive meshing that re-meshes the geometry once the distortion reaching the set threshold could be potentially used for addressing this challenge.

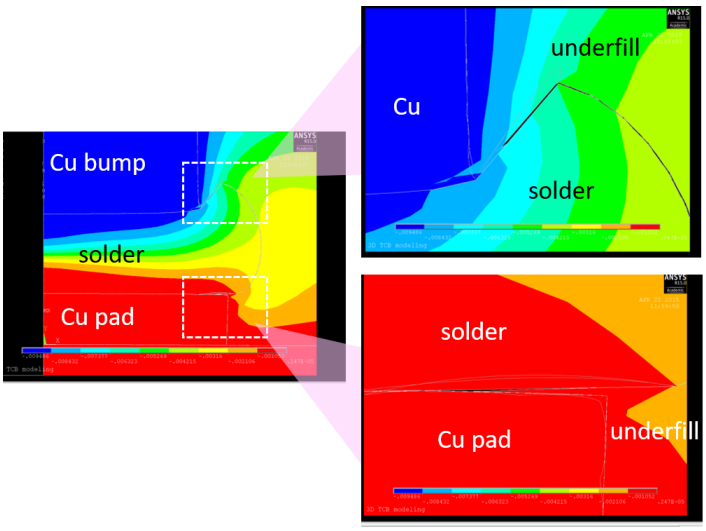


Figure 33. The delamination of NCP and detachment of solder modeled with implementing the contact element.

3.2.3 Process optimization and model justification

To establish the previous model as a design tool for assembly, the model's predictions need to be experimentally validated. It is especially critical that the temperature in solder joints be predicted as accurately as possible so the interfacial reaction may be finely controlled with the designed assembly profiles. The real-time temperature in off-chip interconnections can be measured with the experimental setup of Fig. 34(a), where a 50μm-thick adhesive K-type thermocouple was embedded in the pre-applied underfill layer of a die-to-substrate assembly. Glass packages with three different electrical designs and stack-ups were considered, including 2- and 4-metal-layer substrates with a 100μm-thick core, and a 2-metal-layer substrate with a 200μm-thick core. Assembly trials were carried out on the Finetech Matrix flip-chip bonder with a stage temperature of 70°C and varying thermal profiles on the tool head, as in the model. The measured temperatures for each

package are reported in Fig. 34(b). The observed trends correlate well with the modeling results. Indeed, in the 100µm-thick glass package with 2 metal layers, the temperature in the solder just about exceeded its melting point with 244°C measured with a tool heat temperature of 400°C. A thicker substrate with the same metal loading predictably yielded higher temperatures. The maximum temperature measured for the 4-metal-layer substrate was of only 180°C, closely matching the model's predictions.

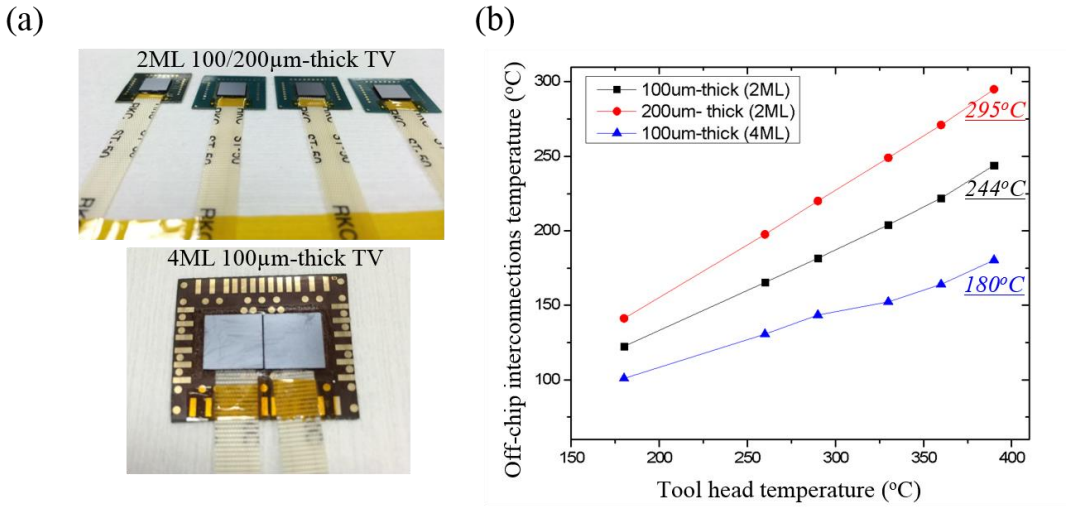


Figure 34. (a) The experimental setup for temperature measurement, and (b) the plot of measured temperatures of off-chip interconnections versus the tool head temperature.

To better understand the effect of the core thickness on the package thermal behavior in TC bonding, a parametric study using TV2 organic substrates with core thicknesses of 100µm, 400µm and 800µm was completed. The details of the test vehicle was described in Section 3.1.2. A filler-free B-stageable no-flow underfill (BNUF) by Namics Corporation was used in this study to control the bump shape and lateral spreading under thermocompression. This material was selected instead of NCP as NCPs typically have high filler loadings, giving high risks of filler entrapment that may interfere with the

interfacial reactions and compromise the results. A thin layer of BNUF was applied on the substrate, covering the bonding site area, then B-staged at 70℃ for 1h. The stage was once again stage was kept at 70℃, while temperature profiles with varying peak temperatures of 350℃, 370℃ and 390℃ were set on die side with a 5s dwell time.

Cross-sections of resulting assemblies are shown in Fig. 35. Ideal metallurgical bonding is accompanied by solder collapse and formation of a continuous intermetallic layer at the interface between solder and substrate pad. The volume of intermetallics formed at this interface, circled in the cross-sections of Fig. 35, and solder collapse were, therefore, used to quickly and qualitatively evaluate the bonding conditions for each substrate. As temperature gradients can be established more easily through thicker substrates, ideal metallurgical bonding was observed with the 800μm-thick substrate in all conditions, judging from the substantial solder collapse and intermetallic growth. With reduction in substrate thickness to 400μm, adequate bonding could now only be achieved with a tool head peak temperature of 390℃. Intermetallics were solely formed in discrete locations with a tool head peak temperature of 350℃ and below, indicating poor solder wetting. Intermetallics were hardly formed on the 100μm-thick substrate, regardless of the bonding conditions, indicating that the temperature of the interconnections was never sufficient to melt the bulk of the solder. Modeling predicted a maximum temperature of 232℃ with such a package and a tool head peak temperature set as 400℃, which is in good accordance with these experimental results.

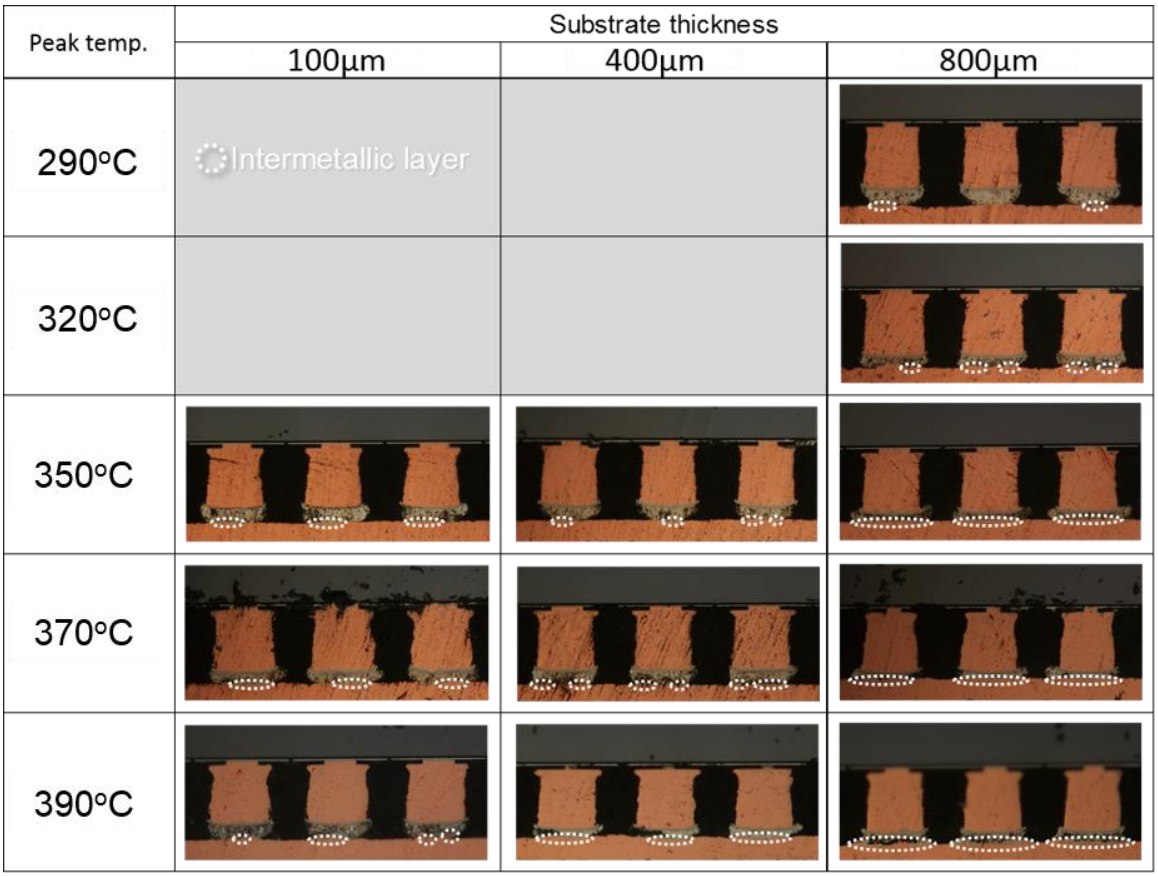


Figure 35. Parametric study with different substrate thicknesses and tool head peak temperatures.

Now that interactions with the bonder and effect of package design have been clarified, the only remaining component is to understand the dynamic interaction between heating and force profiles applied in TC bonding and the curing kinetics of the NCP material. The gelation point of NCP is highly dependent on the heating rate, and shifts to higher temperature with increasing temperature ramp rates [98]. Modeling of the NCP curing behavior as a function of the heating rate provided by Namics Corporation is presented in Fig. 36 to illustrate this mechanism. A jump in gelation point from around 150℃ to 230℃ was observed by increasing the ramp rate from 2K/s to 200K/s. Such conditions correspond to the typical heating rates with lab-scale and production tools,

respectively, showing the criticality of using production equipment to qualify pre-applied materials from their development phase. TC-NCP assembly trials were conducted with a 300°C tool head peak temperature and applied force of 15N, varying only the heating rate, from 2K/s to 200K/s. The previous TV1 at 50µm peripheral pitch was reused for this evaluation, this time assembled on the 2-metal-layer 100µm-thick glass substrate. Cross-sections of assemblies in these conditions are shown in Fig. 37. With a 200K/s ramp rate, NCP cures close to the solder melting point and fails to properly confine the solder, resulting in excessive collapse and overwetting. On the other extreme, NCP cured much before solder melted with a 2K/s ramp rate. The cured NCP prevents solder from wetting on the side of the Cu trace as desired in standard bump-on-trace design. Ideal joint shape was obtained with a heating rate of 100K/s for this material system. Fourier transform infrared spectroscopy (FT-IR) was used to quantitatively analyze the cure degree of NCP as a function of the heating rate. Based on the cross-link mechanism of acrylic-type resins, the intensity ratio between vinyl group (~1650 cm^{-1}) and benzene C-H group (~1500 cm^{-1}) can be used as an indicator of the cure degree. Results from this analysis are shown in Fig. 38. Non- and fully-cured NCP after 3h at 165°C were used as references. The absence of vinyl group found in fully-cured NCP indicates completion of the cross-linking mechanism. This peak is however still present when heating at 200K/s, desirable to maximize the assembly throughput, which means that this material could not reach the wanted high cure degree in these conditions. The qualified NCP material is still in development stage and its composition is currently being optimized for high-speed bonding.

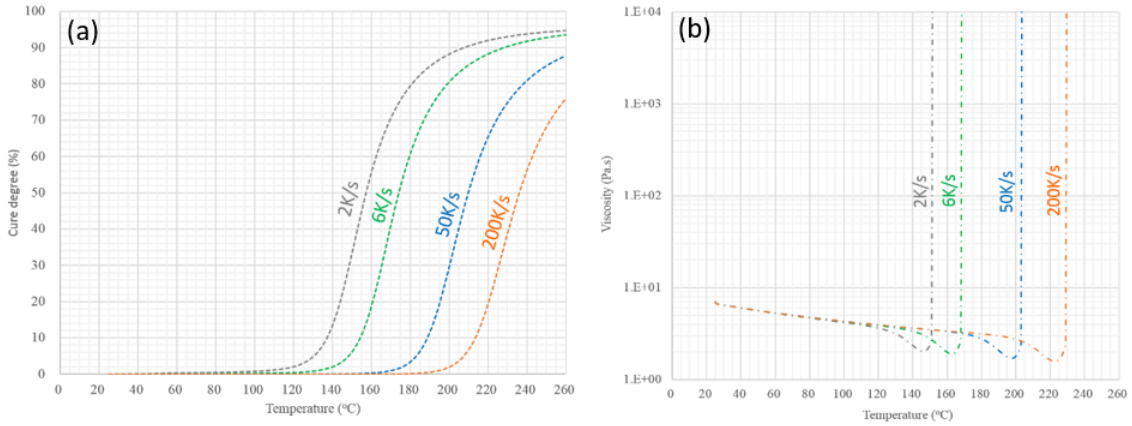


Figure 36. The simulation of (a) cure degree and (b) viscosity versus temperature, with different heat ramp rate. (Courtesy of Namics Corporation)

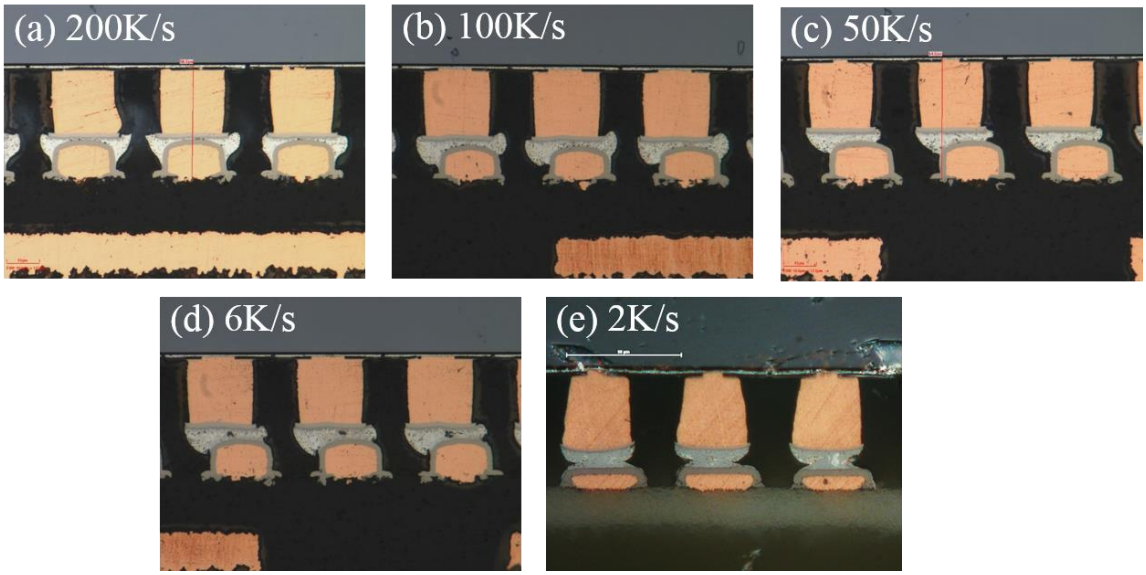


Figure 37. The cross-sections of assemblies bonded with (a) 200K/s (b)100K/s (c) 50K/s (d) 6K/s and (e) 2K/s ramp rate.

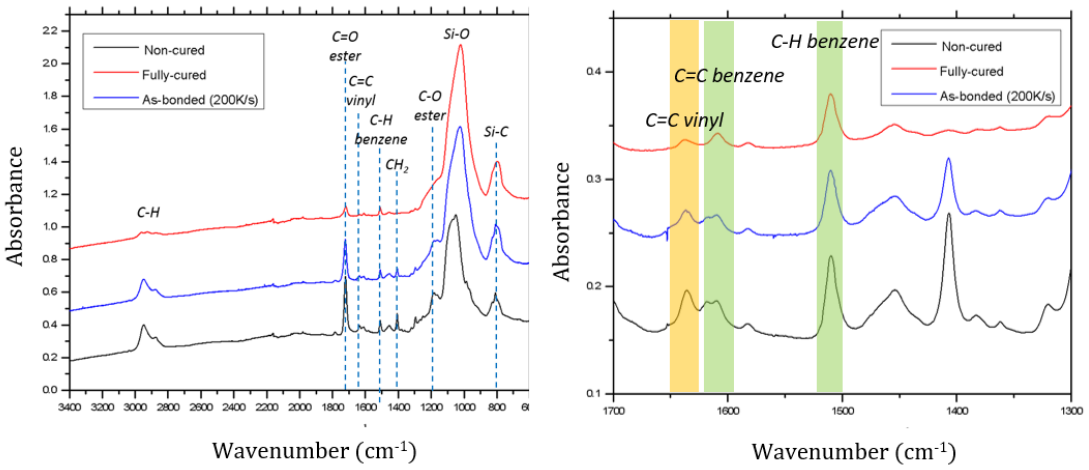


Figure 38. The FT-IR spectrums of non-cured and fully-cured NCP material, comparing with the one as-bonded through TC-NCP process with 200K/s ramp rate.

This task provided a fundamental understanding of the complex synergy between tool, materials, electrical design and process conditions in TC-NCP bonding. Based on excellent model-experiment correlation, the developed modeling approach can confidently be used to design thermal and force profiles and narrow down process conditions for a given test vehicle. This method enabled the development and demonstration of TC-NCP on ultra-thin glass substrates, and was successfully applied to several prototypes, including a single-chip application processor BGA package and a 2.5D high-performance glass interposer, as showed in Fig. 39(a) and (b).

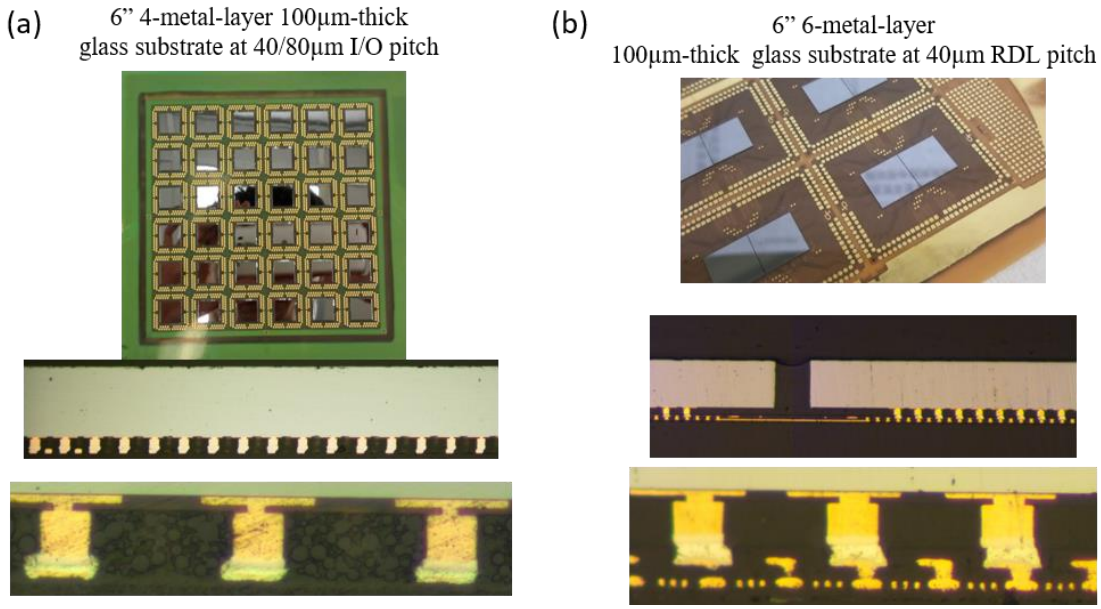


Figure 39. The pictures of (a) single-chip application processor BGA package, and (b) a 2.5D high-performance glass interposer

3.2.4 Summary of design of thermocompression bonding with nonconductive paste

In this section, a co-design of thermocompression bonding process with pre-applied underfill development was demonstrated, improving the state-of-art Cu pillar interconnections into finer pitch application. A full package thermal modeling involving the considerations of BMVs, TPVs, multi-layered routings and the thermal interface between package and TCB tool was conducted to clarify the real temperature distribution once the nominal temperatures were set. With the same tool head temperature, a significant temperature drop from 232℃ to 178℃ was found at the solder when being assembled with four metal-layered 100μm-thick substrate, implying more difficulties for the off-chip interconnects reaching the ideal reflow temperature with ultra-thin substrates, especially with high density of vias and routing layers. With the real temperature distribution, the guidelines of TCB condition for solder collapse control and stress management then can be provided by the multiphysics process modeling with stepwise solving. A 5μm increment of solder collapse was predicted by increasing the temperature ramp from 6K/s to 200K/s, caused by the shift of gelation point toward higher temperature. A NCP material with rapid curing kinetics is required to match the trend of TCB tool capability. Some assembly trials with different thickness substrates and temperature ramp rates were then conducted to verify the modeling results. A solid understanding of TC-NCP process was built from this research task, contributing to the design of assembly process for other research tasks in this thesis.

CHAPTER 4. INTERMETALLICS CONTROL WITH ULTRATHIN SURFACE FINISH

The primary objective of this task is to optimize the Cu microbump system, focusing on surface finish metallurgy, to improve the scalability of pitch size with reduced solder height. A novel electroless Pd (EP) and electroless Pd – autocatalytic Au (EPAG) finishes, recently developed by Atotech GmbH, will be introduced in Section 4.1 as the key innovation of this study. The study then will start with the standard Cu microbump with Ni barrier layer and then move to a Ni-free interconnections with less than 10μm solder height. Various compositions of EP and EPAG were evaluated and compared to standard ENEPIG in terms of wettability, bond strength and thermomechanical reliability to identify the optimal composition to achieve the aforementioned objectives.

4.1 Design of electroless Pd autocatalytic gold (EPAG) surface for controlled interfacial reaction with high performance packages

4.1.1 Deposition test and optimization for Au/Pd embrittlement prevention

To achieve the emerging needs of high performance electronic packages, the next generation surface finish needs to be developed with some specialties, such as 1) compatibility to high density Cu routings with sub-10μnm spacing; 2) Ni-free ultrathin layer for high frequency; 3) controlled interfacial reaction with reduced solder height for high reliability.

To satisfy the first two needs, a deposition test was conducted with EPAG and ENEPIG, as the benchmark. The deposition was accurately controlled with the horizontal

plating line set in Atotech GmbH, Berlin, Germany. Fig. 40(a) and (b) shows the result of depositing trial with a thin ENEPIG, composed of 0.15μm Ni / 0.05μm Pd / 0.05μm Au, and an EPAG, composed of 0.10μm Pd / 0.06μm Au, respectively. With a spacing of 15μm, an extraneous plating was found with thin ENEPIG, potentially caused by overactive activation, unstable electroless Ni bath, high concentrated catalyst or elevated deposition temperature. Though the process optimization has kept proceeding in industry, this challenge by far could not be completed addressed. Theoretically, the outward detached colloidal nickels from the plating front should be inactivated by the stabilizers, such as sulfur-containing organic compound or heavy inorganic cations. However, with such fine spacing, those colloidal nickels would tend to stay within the fine spacing without sufficient coordination with stabilizers. A "self-propagation reaction" could be triggered since those tiny colloid nickels gain more deposition momentum than the desired plating surface, which results in the extraneous plating with Ni flakes. With the proposed EPAG surface, an ideal deposition can be achieved without extraneous plating. The ultrathin coating enables sufficient interaction between colloid ions and stabilizer, which reduces the precipitation grew from the detached colloid ions. Referred to the Cyclic Voltammogram (CV) test, the reduced deposition rate and electrochemical potential of using formic-acid based reducer instead of hypophosphite also inhibits the risk of overactived deposition.

A high accuracy of routing dimensional control is critical for high frequency digital electronics and analog radio-frequency applications. The analysis of dimensional deviation caused by surface finish was conducted with Olympus LEXT laser confocal microscope, as showed in Fig. 41. With the same substrate of TV2, the neighboring Cu traces, with an

initial width and space of 20μm and 30μm, were bridged and thicken to 35-40μm if being applied with standard ENEPIG. A compensation design that takes the growing thickness through deposition into account is infeasible, since a cleaning, microetching process was normally applied before deposition, and the deposition rate is reported as feature dependent. The nano-scaled EPAG surface indeed stands out with improved routing dimensional control, as described in Fig. 41(b). The dimensional deviation caused by EPAG deposition is expected to be less than 0.2μm, and has no risk of extraneous plating.

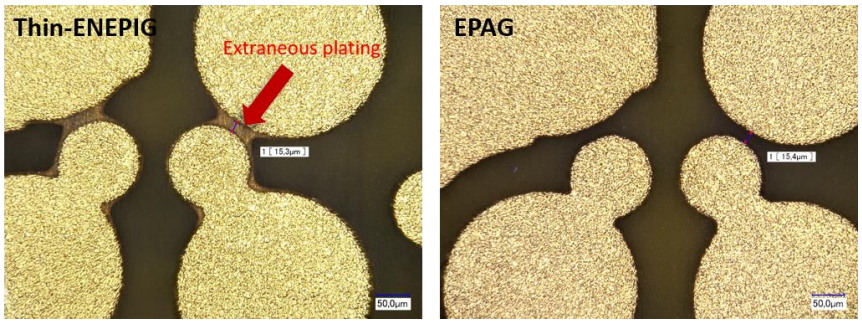


Figure 40. The deposition test of thin-ENEPIG and EPAG with a 15μm spacing.

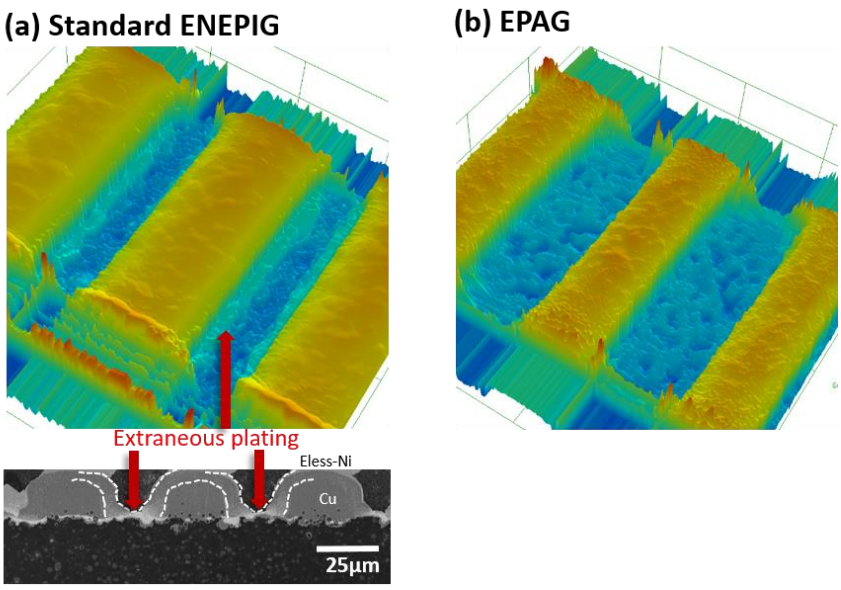


Figure 41. The profile of (a) standard ENEPIG, or (b) EPAG coated Cu traces measured with laser confocal microscope.

Regarding to the third need, the surface finish needs to be well designed for ideal intermetallic composition and corresponds to the reduced solder volume. The Au or Pd embrittlement originated from the brittle (Au, Pd)Sn_4 intermetallic has been considered as the most critical reliability concern with those Au-based surface finishings. The traditional approach in industry of preventing the embrittlement is limiting the Au or Pd concentration lower than 0.1wt%. However, based on Equation 2, only a maximum 4nm Au layer can apply when the solder height is reduced to 10μm. The maximum Au thickness is given by Equation 2:

$$t_{Au} = \frac{0.1\rho_{Sn}V_{Sn}}{0.9\rho_{Au}A} \quad (2)$$

where ρ is the density, V_{Sn} is the solder volume, A is the wetted area, and t is the layer thickness. However, the implementation of such thin Au layer was prohibited since a minimal Au layer is required to achieve a dense coated layer and full coverage. The alternative solution of preventing Au embrittlement needs to be designed more sophisticatedly with the perspectives of interfacial reaction. Within the most common intermetallics formed with solder, Cu_6Sn_5 has been reported as an Au reservoir, storing up to 24.3 at% Au concentration. This Cu_6Sn_5 could be enabled by the proposed EPAG surface finish since the lack of Ni diffusion barrier on the substrate side. In the design of experiment, a 2μm-thick Cu_6Sn_5 was assumed to form on each of the growing fronts through the TC-NCP process. A maximum Au thickness then could be calculated based on the solubility of Au in $(Cu, Au)_6Sn_5$. As predicted, a 85nm-thick Au layer was believed to be dissolved into $(Cu, Au)_6Sn_5$ layer and the Au embrittlement related to $AuSn_4$ thus could be prevented because of the shortage of Au source. Though this calculation is highly simplified, since multiple elements including Cu, Sn, Ni, Au and Pd can still shift the thermodynamic equilibrium, this provides the starting point of the design of experiment with a solid theoretic basis. In this chapter, two different solder microbumps were used, including one standard Cu microbump with 15μm-thick solder and Ni barrier layer, and another of Ni-free microbump with 10μm-thick solder. The plated surface finish compositions for each scenario are summarized in Table 8. As showed, a wider composition range was first set for standard Cu microbumps, since an excessive amount of unreacted solder was expected to share parts of the Au/Pd atoms after assembly. With the case of 10μm-thick solder, the formed joints were expected to be mainly composed of intermetallics. Therefore, a narrowed composition range is selected. Surface finish plating

was performed by Atotech GmbH for a precise control of the plated composition, using the Pallabond Pd chemistry for EP, Pallabond Pd/Au for EPAG, and Aurotech CNN/PD Tech PC/Aurotech SF Plus for ENEPIG. The Fisher XRF was used for thickness measurement, and the mean value and standard deviation of each layer was also summarized in Table 8.

Table 8. Summary of evaluated surface finish compositions.

			Phase I ***Standard Cu Microbump***	***Phase II*** ***Ultrashort Cu Microbump***	***Mean value***	***Standard deviation***
Bump structure			15µm SnAg/2µm Ni/30µm Cu	10µm SnAg/10µm Cu		
Surface finish compositions	EPAG	EPAG-A	Pd 50nm / Au 50nm	Pd 50nm / Au 50nm	Pd 61nm / Au 67nm	Pd 3nm / Au 3nm
		EPAG-B	Pd 100nm / Au 50nm	Pd 100nm / Au 50nm	Pd 119nm / Au 50nm	Pd 6nm / Au 2nm
		EPAG-C	Pd 100nm / Au 100nm		Pd 128nm / Au 101nm	Pd 8nm / Au 4nm
		EPAG-D	Pd 150nm / Au 50nm		Pd 152nm / Au 51nm	Pd 10nm / Au 4nm
	EP	EP-A	Pd 50nm	Pd 50nm	Pd 55nm	Pd 4nm
		EP-B	Pd 100nm	Pd 100nm	Pd 110nm	Pd 2nm
		EP-C	Pd 150nm		Pd 149nm	Pd 3nm
	ENEPIG	ENEPIG	Ni 4µm/Pd 50nm/Au 50nm		Ni 7.3µm / Pd 50nm/ Au 51nm	Ni 57nm / Pd 4nm/ Au 2nm

4.1.2 Solder wettability evaluation

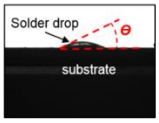
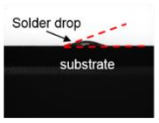
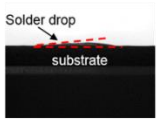
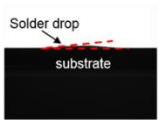
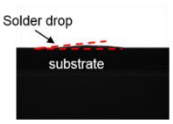
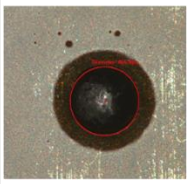
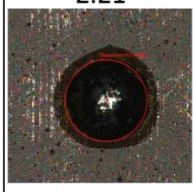
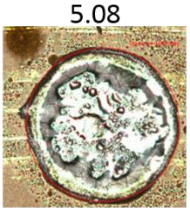
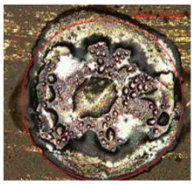
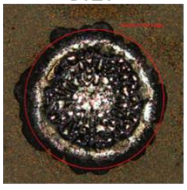
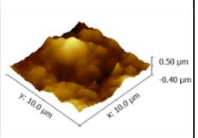
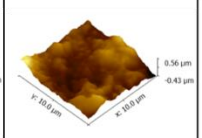
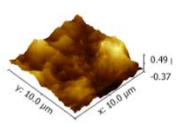
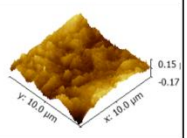
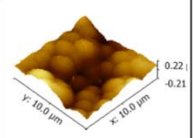
Sessile drop test samples were prepared by reflow of SAC387 (Sn 3.8wt% Ag 0.7wt% Cu) solder balls, 250µm in diameter, on all surface finishes for comparative study of solder wettability. The reflow was performed at a 260°C peak temperature, maintained for 1min, with no-clean liquid flux. A Rame-hart Model 250 goniometer was used to measure the contact angle between solder and substrate metallization. The solder spread was also evaluated with a Zeta 3D optical profilometer. The contact angle measurements, as well as the ratio of wetted area (r) to initial solder diameter (r_o), were used to quantify solder wettability on the investigated finishes. Results of these evaluations are reported in Table 9.

Ideal wettability was observed with ENEPIG and all EPAG compositions, nearly twice greater than with EP finishes. As the Pd content is kept same in, respectively, A and B variations of EPAG and EP, wettability was confirmed mostly governed by the topmost metallic layer, which instantly reacts with the solder. Solder wettability on a given metallic surface is controlled by two prevailing mechanisms: 1) solubility of the reacted metal in solder, and 2) reaction rates of intermetallic formation [99]. Fast dissolution is believed to facilitate solder lateral spreading, while vertical chemical reactions involved in intermetallic formation act as a competing mechanism, impeding lateral driving forces, thus limiting solder spread. Since Au has higher solubility than Pd in solders, but both have fast formation rates of $AuSn_4$ and $PdSn_4$, worse wettability was obtained with EP finishes compared to EPAG, regardless of their composition.

Wettability on EP surfaces was also found highly dependent on the Pd thickness, with improved wettability obtained for EP-B with 100nm Pd as compared to EP-A with 50nm Pd. Considering the topmost metal is in both cases Pd, and the thin Pd layers could be completely dissolved in solder, neither solubility nor intermetallic formation can explain this behavior. However, solder flowability is also conditioned by surface roughness due to capillary-driven flow kinetics [100, 101]. Surface roughness measurements were therefore carried out by atomic force microscopy (AFM) for each surface finish, as shown in Table 9. ENEPIG presented the smoothest surface with a Ra of 61.2nm, while similar higher Ra values, ranging from 94.5nm to 104.9nm, were obtained for EPAG and EP finishes regardless of their composition. Similar wettability of EPAG and ENEPIG indicates that surface roughness did not significantly affect wettability on Au surfaces, rather dominated by the reaction between Au and molten solder. Likewise, surface roughness cannot account

for the discrepancies in wettability observed between EPAG and EP, primarily attributed to the higher solubility of Au in solders, nor between the EP compositions.

Table 9. The solder wettability tests through contact angel measurement and solder sessile drop test. And the surface roughness measured by AFM.

	EP-A	EP-B	EPAG-A	EPAG-B	ENEPIG
Contact angle	25.7° 	18.3° 	6.7° 	6.5° 	6.5° 
Solder ball drop (K=r/r°)	1.87 	2.21 	5.08 	5.15 	5.17 
AFM (Ra)	94.9nm 	104.9nm 	98.5nm 	94.5nm 	61.2nm 

To understand the effect of Pd thickness on wettability, X-ray photoelectron spectroscopy (XPS) was used to identify the composition of the Pd layer within a 10nm depth. The observed Pd 3d and Pd 3p peaks confirm both as-plated EP-A and EP-B surfaces as pure Pd metal. During the reflow process required to form the sessile drop test samples, the Pd surfaces were actually annealed in the slow temperature ramp-up to 230℃ at 2K/s, prior to the solder reaching its melting point and initiating the reaction. To assess the effect of such annealing, EP-A and EP-B substrates were reflowed at 200℃ peak temperature for 1min and again subjected to XPS characterization. The results of Fig. 42 suggest that the surface the solder actually wetted on was indeed modified by this high-temperature storage.

For all EP surfaces, peaks of Pd 3d3/2 and Pd 3d5/2 were found at 340.3 eV and 335 eV, respectively, indicating that Pd did remain in a pure metal state, without oxidation. However, the EP-A surface presented peaks of Cu 2p1/2 and Cu 2p3/2 at 952.3 eV and 932.1 eV, respectively. While the Pd layer remained technically unchanged, the chemical shift with apparition of Cu 2p peaks after annealing indicates that Cu can easily diffuse through the entire 50nm Pd thickness and get oxidized to form Cu_2O. This copper oxide is believed to deteriorate solder wettability. Moreover, very thin metal layers formed with electroless processes, particularly electroless nickel, tend to form highly-porous coatings. In the EP-A composition with only 50nm Pd thickness, inherent porosity is expected to provide more surface diffusion paths for Cu, further aggravating oxidation risks and subsequently degrading wettability.

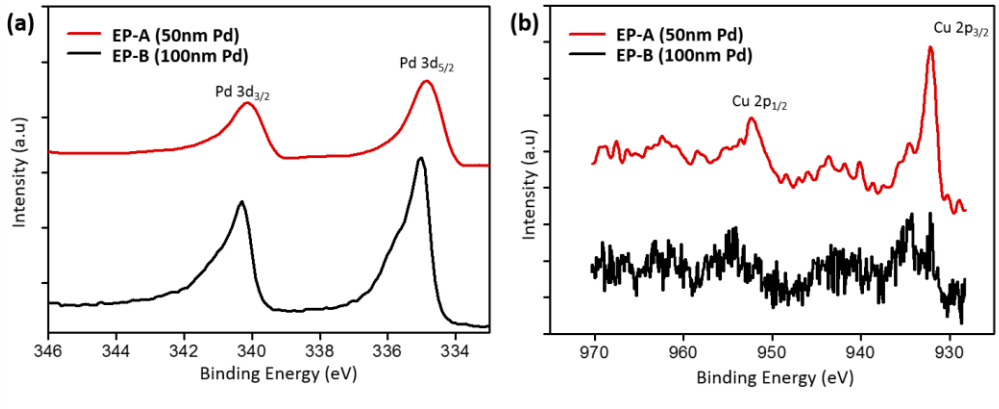


Figure 42. The XPS of (a) Pd 3d and (b) Cu 2p peaks, measured with EP-A and EP-B surfaces after thermal annealing for 1min.

4.2 Phase I: Assembly with standard Cu microbump with Ni barrier

In this section, the TV2 with designed composition as listed in Table 8 was assembled with the standard Cu microbumps, having a Ni diffusion barrier layer on the

bump side and a solder height of 15µm. The microstructure will be first analyzed and followed by thermomechanical reliability test. This study was projected to providing the benchmark of current Cu microbump technology before scaling down the solder height and pitch size, which will be covered in Section 4.3.

4.2.1 Microstructure analysis through high-temperature storage

Based on the understandings built from the studies of TC-NCP process, as described in Section 3.2, the samples in this section were assembled with the optimal bonding profile of having a 300℃ peak temperature for 3s and a pressure of 40MPa. A NCP material was used and bonded with a temperature ramp rate of 50K/s.

The SEM backscattered electron images (BEI) of the as-bonded Cu pillar joints and that through 500h HTS are shown in Fig. 43 and Fig. 44. With ENEPIG, a dominant amount of (Pd, Au, Ni)Sn_4 was found growing from the substrate interface after assembly. This could be well explained by the Sn-rich corner of Pd-Ni-Sn ternary phase diagram [102], in which the solubility of Pd in Sn was found dramatically decreased while being doped with 0.15 wt% Ni atoms. This reduced solubility prevents the precipitated (Pd, Au, Ni)Sn_4 from spalling and dissolving back into the unreacted solder. After 500h HTS, the entire joint was composed of (Pd, Au, Ni)Sn_4, and a layer of $(Ni, Cu)_3Sn_4$ was observed on both top and bottom interfaces. Even some studies suggested that the $PdSn_4$ would tend to coarsen and gradually dissolve through thermal aging or multiple reflow [103], but this would only be applied if massive unreacted solder was still available through entire experiment. Comparing to the solder height of 60µm or 1200µm, the initial solder in this study is less than 15µm, which is apparently less enough to accommodate all the Pd atoms.

In addition, the (Ni, $Cu_3)_4Sn$ was the only another intermetallic formed on the interface since the joint was confined by the Ni diffusion barriers from both die and substrate side, which contributes negligible Pd solubility. Summing up the effects of limited solder volume and formed (Ni, $Cu_3)_4Sn$, the Pd atoms could only stay as the phase of (Pd, Au, $Ni)Sn_4$ and keep growing with the Ni source from (Ni, $Cu)_3Sn_4$. The Cu concentration within (Ni, $Cu)_3Sn_4$ ranged of 3.0 - 4.6 at% (atomic percent) , which is believed to be sourced from the Cu trace beneath the electroless Ni that generally has comparatively porous or columnar morphology with high grain boundary diffusion rate. With the image of ENEPIG after 500h HTS, the crack found at the right corner of joint implies the brittleness of such joints composed by (Pd, Au, $Ni)Sn_4$. The similar cracks were found with all the bonded joints even only one was choose for demonstration.

A similar behavior was found with EP-A, B and C. The $PdSn_4$ precipitated through the substrate interface after bonding, and the intermetallics underneath transferred form (Cu, $Ni)_6Sn_5$ to (Cu, $Ni)_3Sn$ if having Pd thickness over 100nm. With the existence of (Cu, $Ni)_6Sn_5$ and increased amount of unreacted solder after bonding, the thermodynamic equilibrium switched to forming the full-intermellic joint mainly with (Cu, $Ni)_6Sn_5$. With the composition analysis with XEDS, the Ni concentration in (Cu, $Ni)_6Sn_5$ ranged within 2.6-5.2 at%, and an exclusive formation of (Pd, Au, $Ni)Sn_4$ as with ENEPIG thus could not proceed with such limited Ni source. Without the role of Ni, the solubility of Pd in Sn could be remained at 0.45 at%, and the massive (Cu, $Ni)_6Sn_5$ could also act as the reservoir of Pd atoms even the solubility was reported less than 1at%. By comparing the images of as-bonded and after 500h HTS, some $PdSn_4$ was dissolved into solder or (Cu, $Ni)_6Sn_5$, and a

higher concentration of Pd, corresponding to EP-C, interfered in the interdiffusion of Sn and Cu, resulting in a reduced growth rate of $(Cu, Ni)_6Sn_5$.

With EPAG surface, as showed in Fig. 44, a significant different of microstructure was found after bonding, in which the aggregated $(Pd, Au)Sn_4$ was observed on the substrate interface with EPAG-B, C and D. With EPAG-A, the $(Cu, Ni)_6Sn_5$ mainly contributed to the joints and some scattered disk-shaped precipitate of $(Au, Pd)Sn_4$ was found within the solder. With the composition analysis with XEDS, the Pd concentration of $(Pd, Au)Sn_4$ with EPAG-B, C and D ranged 15.6-17.9 at%, and the $(Au, Pd)Sn_4$ found in EPAG-A showed an Au concentration close to 20 at%. This result indicates that the brittle $(Pd, Au)Sn_4$ would be expected if having a Pd thickness over 100nm, and the embrittlement is actually less sensitive to the Au thickness since both EPAG-B and EPAG-C perform similar as-bonded microstructure. An interesting finding is that, while EP-A showed a bulky precipitate of $PdSn_4$ on the substrate interface, that potentially risks the bond strength, the additional 50nm-thick Au layer in EPAG-A could change the precipitate to Au-rich $(Au, Pd)Sn_4$ away from the interface. After 500h HTS, all the EPAG assemblies transferred to all-intermetallic interconnections with the main phase of $(Cu, Ni)_6Sn_5$. With the standard Cu microbumps, significant unreacted solder remained after bonding. An active interdiffusion between Cu-Sn, forming thick $(Cu, Ni)_6Sn_5$ and $(Cu, Ni)_3Sn$, thus was predicted, as confirmed in Fig. 44. This $(Cu, Ni)_6Sn_5$ approximately ranged 11-15μm provides enough substitutional space for both Au and Pd, the $(Pd, Au)Sn_4$ initially precipitated on the substrate interface thus dissolved back into unreacted solder first, then $(Cu, Ni)_6Sn_5$ through HTS. Even a similar microstructure was found after HTS, the as-bonded reliability was expected to be more sensitive to the composition of EPAGs and the

corresponding interfacial reaction. The die shear test will be conducted with reduced solder height of 10μm in next Section 4.3.

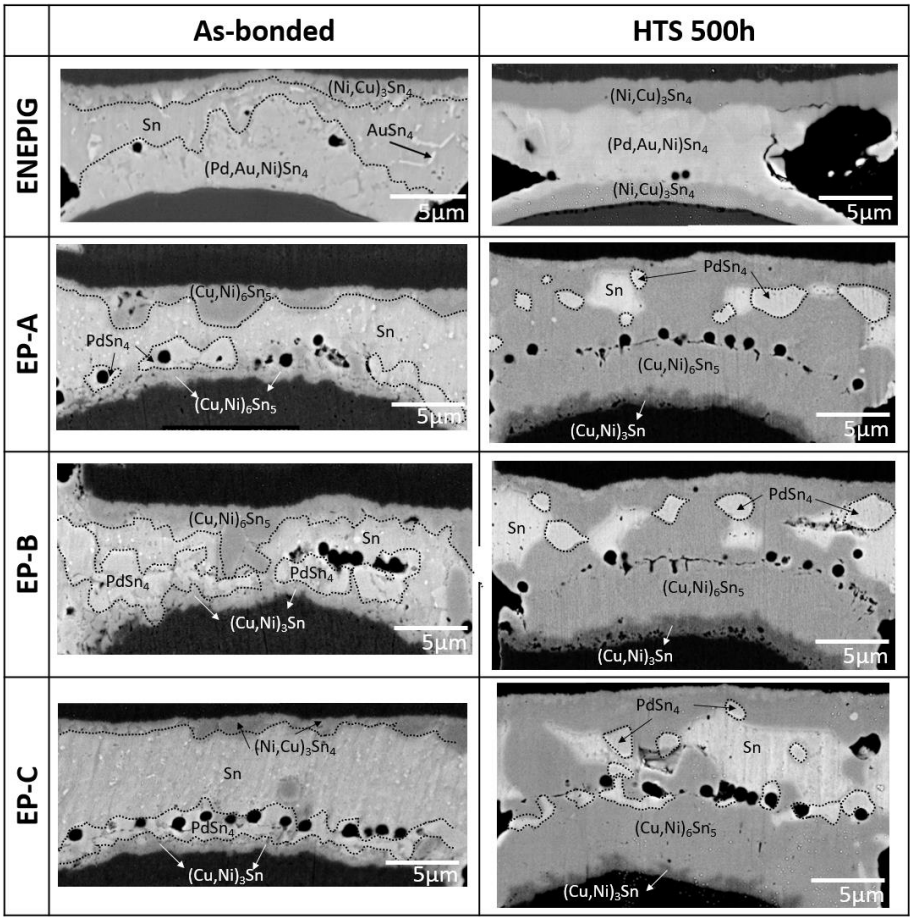


Figure 43. The BEI images of the interfaces through thermal aging at 150°C till 500h with ENEPIG and EPs.

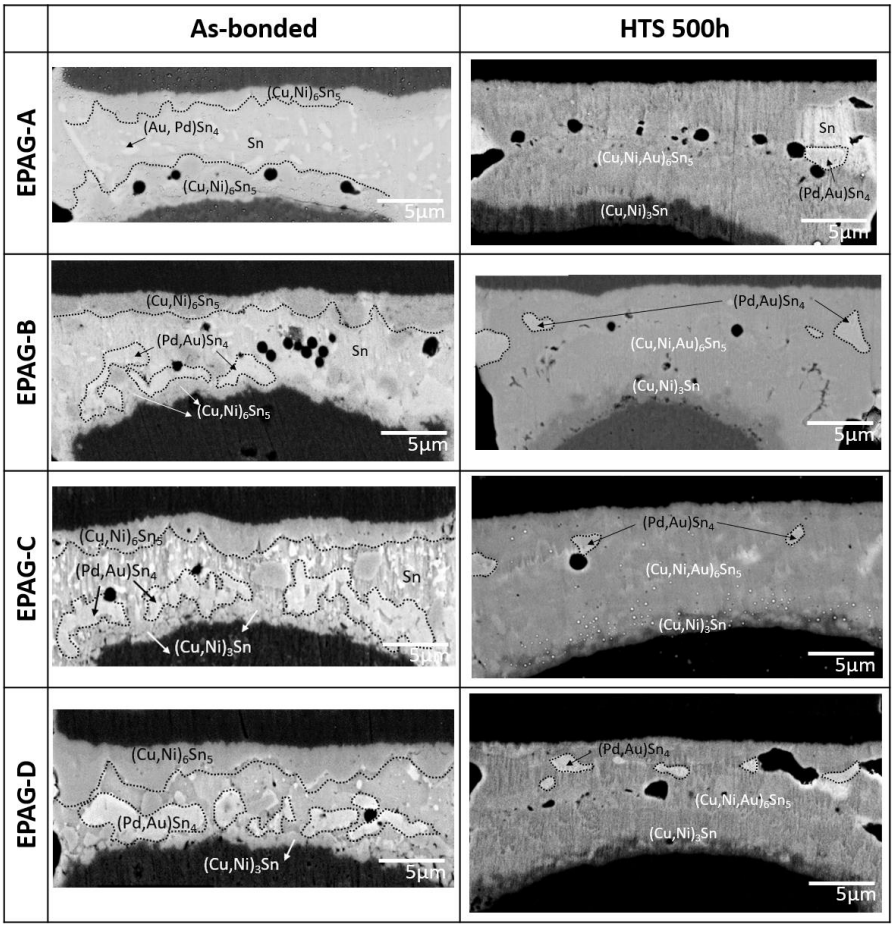


Figure 44. The BEI images of the interfaces through thermal aging at 150°C till 500h with EPAGs.

However, those thick (Cu, Ni)$_6$Sn$_5$ and (Cu, Ni)$_3$Sn brought a concern of serious Cu consumption of the bonded Cu pads. Comparing to ENEPIG that has 4-6μm-thick electroless Ni diffusion barrier and slower Ni-Sn interdiffusion rate, the EPAG surface has compromised the diffusion barrier to enable the nano-scaled coating. An evaluation of Cu consumption was conducted by comparing the Cu pad thickness before and after bonding, and also after 500h HTS. The Cu pad was first measured with Olympus LEXT laser confocal microscope before bonding, and then measured referring to the cross-sectioned SEM images after bonding and HTS. Since the electroplated Cu pad formed an arched top

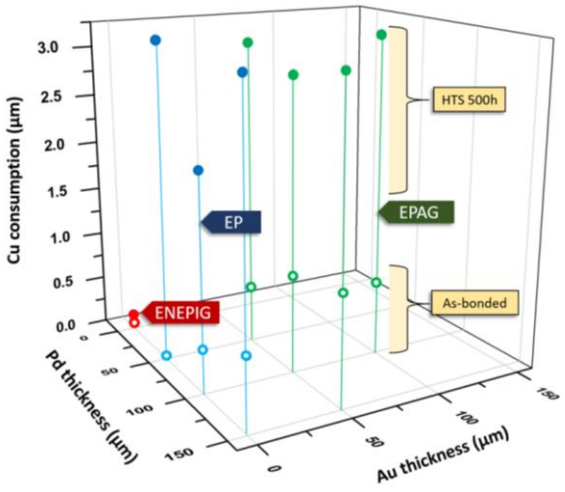
surface, this evaluation was based on the apex-bottom thickness. The Cu consumptions were summarized in Fig. 45, in which the hollow or solid circles represent that of as-bonded or after 500h HTS. As predicted, the ENPEIG showed negligible Cu consumption even after HTS because of the Ni_3Sn_4 and (Pd, Au, Ni)Sn_4 as the major intermetallics. Comparing as-bonded EPAGs and EPs, EPAGs showed higher Cu consumption of 0.59-1.13μm than EPs of 0.03-0.75μm, caused by the enhanced wettability of Au-based top surface. A significant Cu consumption was found with both EPAGs and EPs after 500h HTS, ranged 2.16-3.23μm, without major difference between those different surfaces. It's believed that the EPAGs or EPs were completely dissolved into solder during bonding, and it was the Cu-Sn solid-state interdiffusion was controlling the Cu consumption through HTS. According to the Cu-Sn intermetallic growth model under 150℃ aging, the total thickness of formed intermetallics could be assumed linearly proportional to the square root of aging time since its diffusion-controlled mechanism. The total formed intermetallic's thickness is given by Equation 3 and 4 [104]:

$$x = \sqrt{\widetilde{D}t} \tag{3}$$

$$\widetilde{D} = \widetilde{D}_0 \exp\left(-\frac{Q}{RT}\right) \tag{4}$$

where x is the total thickness of Cu-Sn intermetallics, $\widetilde{D}$ is the interdiffusion coefficient, $\widetilde{D}_0$ is the pre-exponential factor , Q is the activation energy, T is the absolute temperature, R is the gas constant, and t is the aging time. Taken $\widetilde{D}_0$ as 4×10^{11} $\mu m^2/s$ and Q as 138 kJ/mole, the estimated total intermetallic thickness is 2.56μm. Since this number was contributed by two species, Cu_6Sn_5 and Cu_3Sn, and only a single growing front was taken

into account, a simple approximation was made by assuming that the Cu_6Sn_5 thickness was approximately four times than Cu_3Sn, and the growth rate of die and substrate interface is the same. As the result, a 1.02μm-thick Cu_3Sn and a 4.09μm-thick Cu_6Sn_5 was predicted to grow through 500h HTS. The corresponding Cu consumption then could be predicted as 2.16μm by applying the mass conservation theory. Comparing to the measured results list in Fig. 45, this estimation indeed provides a method of predicting the Cu consumption of bonded pads. However, the serious Cu consumption implies the limitation of EPAGs or EPs, in which the thin high density Cu routings widely used in current packaging substrates could be completely dissolved and delaminated. Being bonded with the standard Cu microbumps means that an active interdiffusion of Cu-Sn could be expected since the plenty of solder supply, and the Ni diffusion barrier layer on the bump aggravates the concern since the Cu pad needs to replenish the Cu concentration of solder exclusively. Based on the microstructure analysis in this section, we suggest a Ni-free Cu bump with reduced solder height could be the most promising application of EPAG surface, which will be discussed in Section 4.3.



		Composition	Cu consumption (µm)	
			As-bonded	HTS 500h
EPAG	EPAG-A	Pd 50nm / Au 50nm	0.59	3.11
	EPAG-B	Pd 100nm / Au 50nm	1.00	2.93
	EPAG-C	Pd 100nm / Au 100nm	0.75	3.23
	EPAG-D	Pd 150nm / Au 50nm	1.13	3.10
EP	EP-A	Pd 50nm	0.03	3.20
	EP-B	Pd 100nm	0.45	2.16
	EP-C	Pd 150nm	0.75	3.16
ENEPIG		Ni 4µm/Pd 50nm/Au 50nm	0.07	0.16

Figure 45. The Cu consumption of each surface composition, as-bonded and after 500h HTS at 150°C.

4.2.2 Thermomechanical reliability test

The assemblies were bonded with the same optimal parameters as in Section 4.2.1 for thermomechanical reliability test. Four samples with 64 daisy chains were built for each surface composition, and the as-bonded yield of each composition is: 89% for ENEPIG, 100% for EPAG-A, 98% for EPAG-B, 100% for EPAG-C, 97% for EPAG-D, 98% for EP-A, 97% for EP-B, and 98% for EP-C. The comparatively lower as-bonded yield with ENEPIG could be caused by the different supplier for ENEPIG deposition. The daisy-chain resistances showed a standard deviation of 0.09Ω for ENEPIG, 0.05-0.09Ω for EPAGs, and 0.09-0.15Ω for EPs, in which the higher fluctuation of EPs could be contributed by the non-ideal wettability of EP-A and EP-B. The test assemblies were subjected to liquid-to-liquid thermal shock test at -55°C / 125°C with a rate of 2 cycles per hour, following JEDEC standards. The daisy chain electrical resistances were monitored up to 1000 cycles with a 20% increase in as-bonded resistance used as failure criterion. Fig. 46 shows the photo of bonded assemblies for thermal shock test. Fig. 47 shows the resistances of bonded chains

monitored till 1000 cycles. Based on the FEM modelling and Coffin-Manson equation, the predicted fatigue lifetime ranged 1200-1400 cycles, granted by the high standoff height. The ENEPIG and EPs of more than 100nm Pd thickness showed the unsatisfying lifetime with more than 10% fail percentage within 1000 cycles. This early failure could be explained by the fragile (Pd, Au, Ni)Sn_4 or $PdSn_4$ observed in the as-bonded joints. With EPAGs and EP-A, the stable resistance indicates an improved reliability over standard ENEPIG surface, in which the thermomechanical reliability was likely less sensitive to the nano-scaled change of surface composition due to the relatively higher volume of solder.

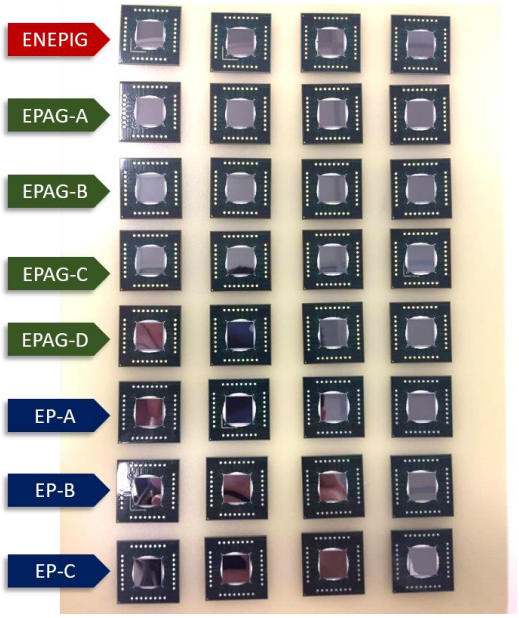


Figure 46. The bonded assemblies with standard Cu microbumps for thermomechanical reliability test.

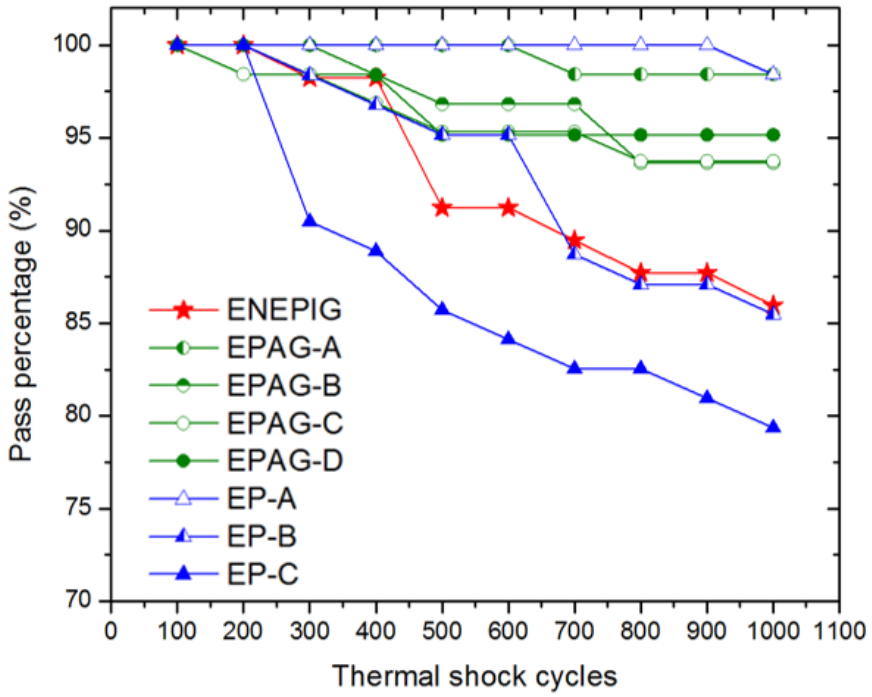


Figure 47. The electrical resistance monitored till 1000 thermal shock cycles. The test is in progress.

4.3 Phase II: Assembly with ultrashort Cu microbump without Ni barrier

In this section, the standard Cu microbumps were scaled down with a Ni-free Cu microbump, having a reduced solder height of 10µm. The TV1 was selected and deposited with the surface compositions summarized in Table 8. The microstructure observed will be compared with Section 4.2, and a comprehensive reliability evaluation of shear test and thermomehancial reliability will follow.

4.3.1 Microstructure analysis through high-temperature storage

In ENEPIG assemblies, a continuous layer of (Au, Pd, Ni)Sn_4 with 3.8 at% of Ni precipitated at the interface between (Cu, Ni, Au)$_6Sn_5$ and solder during assembly.

Comparing to the case of Section 4.2, although the presence of an infinite Cu supply, here provided by the Cu pillars, has been suggested to inhibit Au embrittlement [105], a serious precipitation of (Pd, Au, Ni)Sn_4 was still observed. After thermal aging for 100h, all the initially scattered intermetallics relocated into the continuous (Pd, Au, Ni)Sn_4 layer due to thermodynamic stabilization [106]. Since (Pd, Au, Ni)Sn_4 can continuously form from the Ni supply only, even after full consumption of the Au and Pd contained in ENEPIG [107], a more significant amount of (Pd, Au, Ni)Sn_4 was found after thermal aging. Comparing the results of 500h HTS in Fig. 43 and Fig. 48, the growing rate of (Pd, Au, Ni)Sn_4 was significantly suppressed since the Ni atoms now could only be supplied from the substrate side. In addition, the (Cu, Ni, Au)$_6Sn_5$ but (Ni, Cu)$_3Sn_4$ initially formed at the substrate interface because of the saturated concentration of Cu within the solder, the Ni diffusion flux toward the solder was blocked effectively by this (Cu, Ni, Au)$_6Sn_5$. As the results, the growth of (Pd, Au, Ni)Sn_4 was found slower with the existence of (Cu, Ni, Au)$_6Sn_5$. This (Pd, Au, Ni)Sn_4 layer acted as a barrier impeding interdiffusion between solder and copper from the substrate interface. Consequently, the (Cu, Ni, Au)$_6Sn_5$ layer present at the Cu pillar interface was gradually replaced by (Cu, Ni)$_3$Sn due to the lack of Sn source through 500h of HTS. On the substrate side, the (Cu, Ni, Au)$_6Sn_5$ initially formed at the Ni interface was replaced by (Ni, Cu)$_3Sn_4$ after 100h HTS due to the blockage of the Cu supply from the substrate pads by the continuous (Pd, Cu, Ni)Sn_4 layer.

In as-bonded EP-A/B and EPAG-B assemblies, $PdSn_4$ and (Au, Pd)Sn_4 were observed, respectively. With the significantly reduced solder of 7-8μm, comparing to Section 4.2, the increased concentrations of Au and Pd are of 0.9 at% for 50nm-thick Au, 0.78 at% for 50nm-thick Pd, and 1.56 at% for 100nm-thick Pd. Considering the binary

phase diagrams, these compositions exist in the two-phase field, in which the solvus line separating it from Sn is critical for application of the supersaturation mechanism.

In as-bonded EP-A/B assemblies, a significant amount of $PdSn_4$ was found, since most of the Pd atoms were forced to precipitate during the assembly cool-down phase, at temperatures below the Sn-Pd eutectic point of 230℃. In contrast, the Pd-rich $(Pd_{0.84}, Au_{0.16})Sn_4$ phase was observed in EPAG-B as-bonded assemblies instead of the Au-rich $(Au_x, Pd_{1-x})Sn_4$ phase, which indicates that the embrittlement was predominantly caused by Pd and its role in the interfacial reaction. Solubility of Pd in Sn is relatively low at the eutectic Sn-Pd point of 231℃ [108]. In contrast, the solvus line between Sn and the two-phase field imposes a maximum Au solubility of 0.4 at% in the Sn-Au system at 220℃ [109]. Consequently, majority of the Pd atoms are expelled from the cooled Sn and form Pd-rich intermetallics, in both EP-A/B and EPAG-B assemblies.

Through the HTS up to 500h, The $(Cu, Au, Pd)_6Sn_5$ phase started to dominate the microstructure. As previously mentioned, a sufficient Cu supply can effectively prevent gold embrittlement caused by $AuSn_4$, as the $(Cu, Au)_6Sn_5$ phase can act as a Au reservoir up to 24.3 at% [110, 111]. However, the solubility of Pd in $(Cu, Pd)_6Sn_5$ is limited to less than 1 at% [112]. With a standard Cu microbump, as in Section 4.2, this solubility difference between Pd and Au would be less significant since a 11-15μm-thick Cu_6Sn_5 guarantees a sufficient accommodation for both Au and Pd. However, with a reduced solder height, EPAG-B showed a serious precipitate of $(Pd, Au)Sn_4$ after 500h HTS.

In this research, the embrittlement is most sensitive to the Pd concentration. Introduction of Cu to form $(Cu, Au)_6Sn_5$ can prevent formation of $AuSn_4$ but not of (Pd,

Au)Sn_4. Interestingly, the EP-A finish's 50nm-thick Pd layer induces massive $PdSn_4$ precipitates, while (Pd, Au)Sn_4 was completely suppressed when this same Pd layer is covered by an additional 50nm-thick Au layer, as in EPAG-A. In the case of EPAG-B, where the same 50nm-thick Au layer was overlaid on a thicker 100nm Pd layer, the (Pd, Au)Sn_4 phase reemerged. These findings indicate that with extremely limited solder volumes, 6-7µm in height after assembly, a specific ratio of Au/Pd can effectively stabilize the reacted interface by formation of (Cu, Au, Pd)$_6Sn_5$. The fundamental mechanism is still not fully understood but based on thermodynamics and published prior art, Au and Pd atoms show a high inclination of coupling to reduce the overall Gibbs' free energy [112, 113]. Once Pd atoms tend to be deactivated by Au atoms, formation of (Pd, Au)Sn_4 is possibly suppressed. A specific Au/Pd ratio is required for this coupling effect to occur, as shown with the EPAG-B finish where Au atoms are not sufficient to stabilize all the Pd atoms, some remaining available for $PdSn_4$ formation.

The XEDS mappings of the assemblies after 500h of thermal aging are shown in Fig. 49. The continuous (Au, Pd, Ni)Sn_4 effectively hindered interdiffusion across the connecting layer, and some solder remained unreacted after aging. With EP finishes, highly concentrated Pd indicated $PdSn_4$ precipitation near the interface. Similarly, Pd-rich precipitation of (Pd, Au)Sn_4 was observed with EPAG-B. With the optimal EPAG-A composition of 50nm Pd/50nm Au, a uniform layer of (Cu, Pd, Au)$_6Sn_5$ was formed with no sign of gold embrittlement. Thermomechanical reliability was then studied to confirm the effect of these interfacial reactions on the fatigue life of the resulting interconnections.

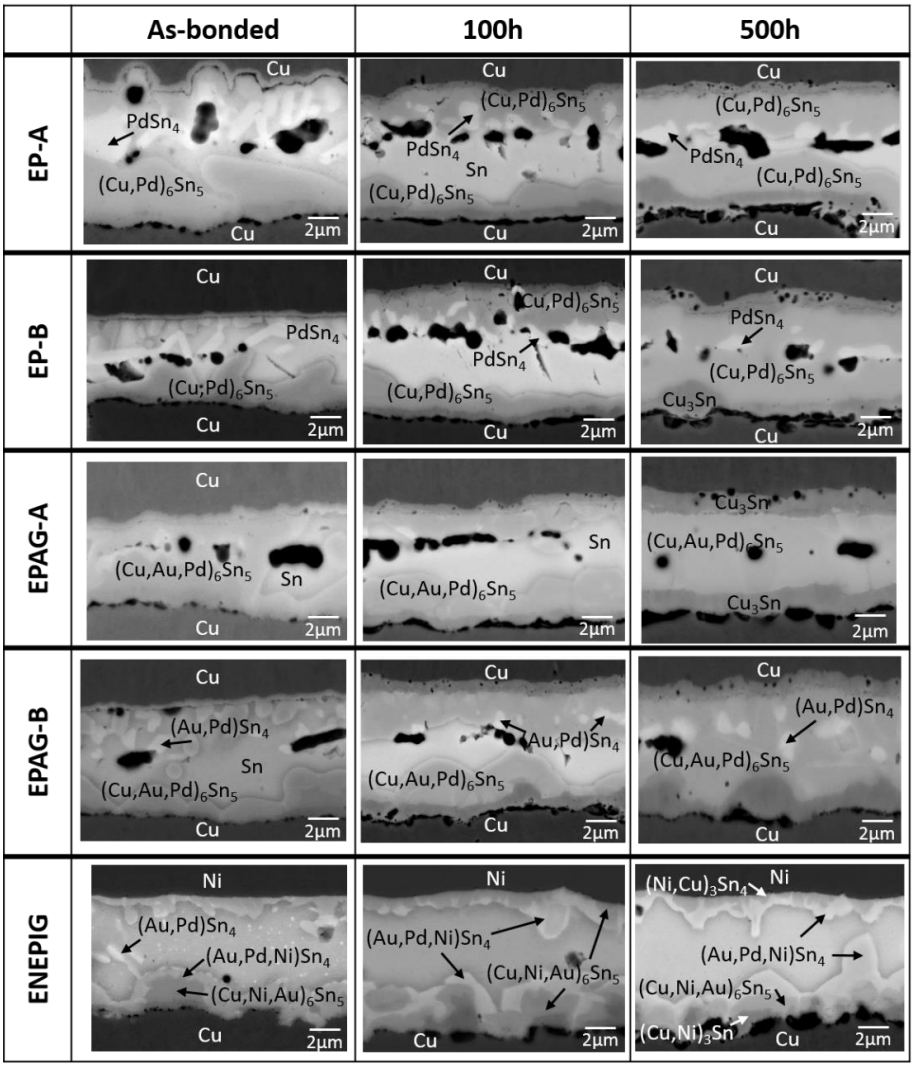


Figure 48. The BEI images of the interfaces through thermal aging at 150°C till 500h.

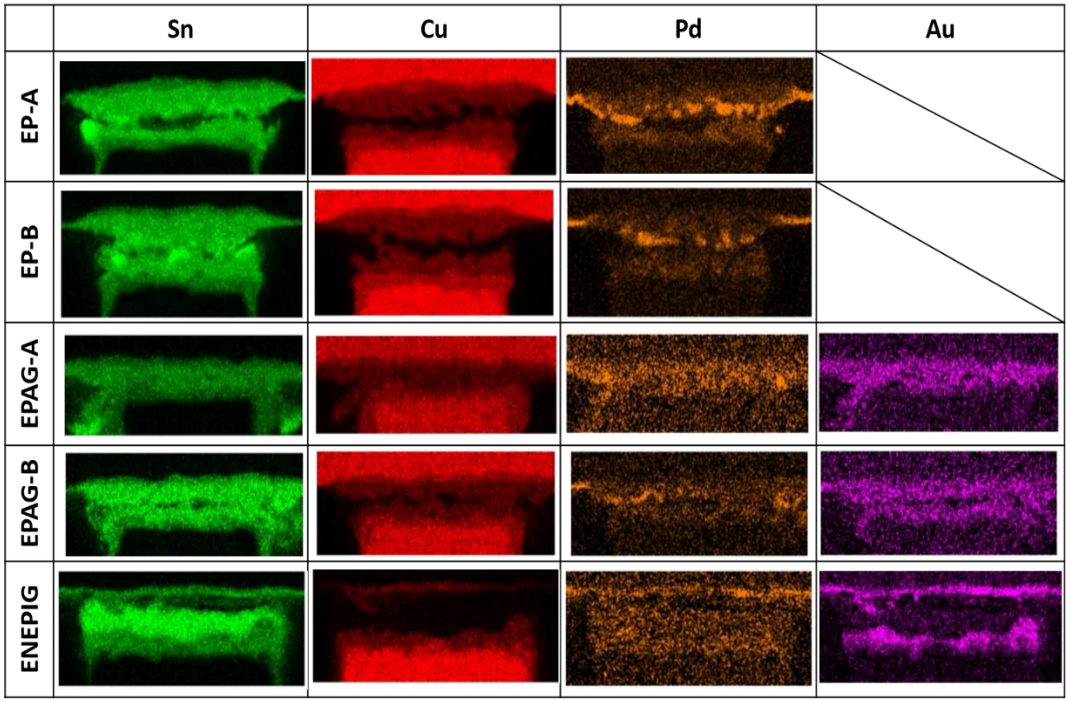


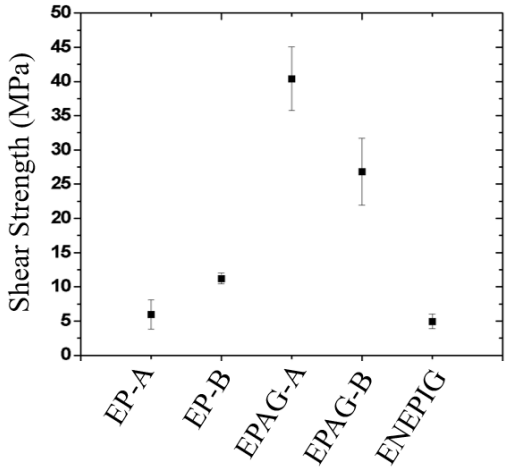
Figure 49. XEDS mappings after 500h of high-temperature storage at 150°C.

4.3.2 Die shear test

Die-shear testing was carried out following the MIL-STD-883G Method 2019.7, using a Dage-Series-400 bond tester with a die-shear cartridge of 10 kgf. The speed of the shear tool was set to 16.0µm/s with a tool height of 5µm from the substrate. Assemblies without underfill were used in this study to directly qualify the bonding strength of Cu pillar interconnections formed on the investigated surface finishes. Twelve samples were built for each surface finish. Shear-strength values in MPa were derived from the maximum loading (kgf) measured right before failure, considering the designed bump diameter and I/O count. The results are summarized in Fig. 50.

Average shear strengths of 5.96MPa and 11.23MPa were achieved with EP-A and EP-B, respectively, dropping to 4.95MPa with ENEPIG. Highest strength of 40.4MPa was

obtained with EPAG-A, falling within expected values for solder-based interconnections, in the 30MPa-60MPa range [114, 115]. These results correlate well with previously explained microstructural evolutions on the different surfaces. With EP-A/B, shear strength is expectedly limited by the fragile rod-like $PdSn_4$ precipitates. The SEM images of the fracture surfaces of ENEPIG and EPAG-A are shown in Fig. 51. ENEPIG assemblies failed by brittle fracture through the fragile interface between solder and $(Cu, Ni, Au)_6Sn_5$ and continuous $(Au, Pd, Ni)Sn_4$ intermetallics, as indicated by the cleavage-type surface observed in Fig. 51(a, b). Improvements in shear strength with EPAG-A were provided by the unique interfacial reaction that led to joints composed of $(Cu, Au, Pd)_6Sn_5$ and solder exclusively, without any intermetallics causing gold embrittlement. The EPAG-A joints ideally failed by ductile fracture through the bulk of the residual solder, as shown in Fig. 51(c, d).



Composition	Average shear strength (MPa)	Standard deviation (MPa)
EP-A	5.96	2.12
EP-B	11.23	0.78
EPAG-A	40.40	4.65
EPAG-B	26.83	4.89
ENEPIG	4.95	1.07

Figure 50. Shear strength of different surface finishes.

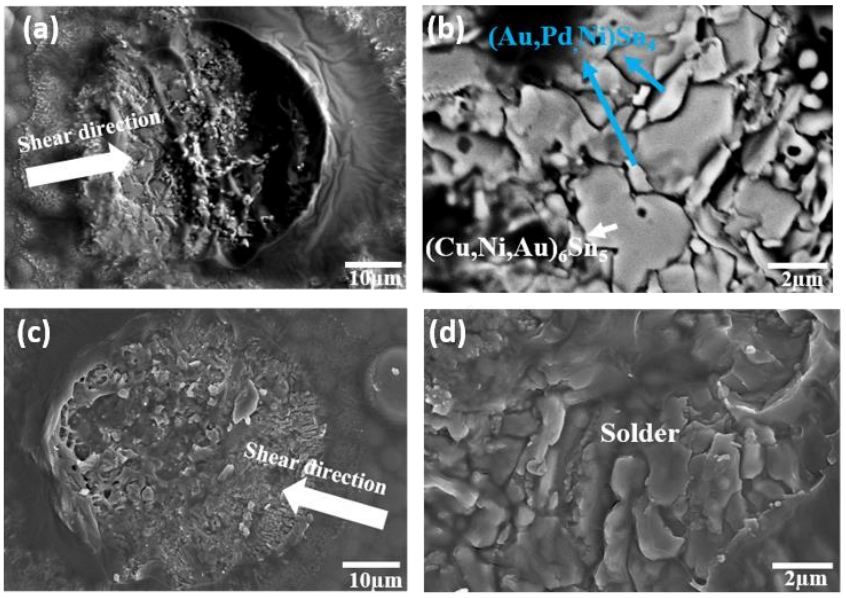


Figure 51. The fracture surfaces of (a, b) ENEPIG, and (c, d) EPAG-A.

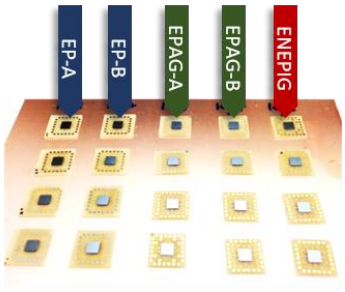
4.3.3 Thermomechanical reliability test

To evaluate the effect of surface finish on thermomechanical reliability of ultra-short Cu pillar interconnections, silicon daisy-chain test dies were assembled onto FR-4 test substrates with the design of TV1. Die-to-substrate assemblies were formed by TC-NCP process as described in Section 3.2. Four samples were built for each surface finish, with a total of 64 measurable daisy chains per variation. The test assemblies were subjected to same test condition as previous phase with standard Cu microbumps, which is a liquid-to-liquid thermal shock test at -55℃ / 125℃ with a rate of 2 cycles per hour, following JEDEC standards. The daisy chain electrical resistances were monitored up to 500 cycles with a 20% increase in as-bonded resistance used as failure criterion. The test samples are shown in Fig. 52(a) with as-bonded assembly yield.

Given the large CTE mismatch between silicon and FR-4 with CTEs of 2.56 and 17.5 ppm/K, respectively, high stress levels concentrated at the intermetallic interfaces and high plastic strains in solders are expected due to the discontinuity in material properties. To estimate the fatigue life of Cu pillar interconnections in this package configuration, a 2D finite element model (FEM) was built in ANSYS following the test vehicle design. Considering the solder collapse observed in cross-sectioned assemblies, a solder height of 6µm instead of the initial 10µm was implemented. Intermetallics were disregarded at this time to simplify the model. The increment in equivalent plastic strain over a thermal shock cycle in the solder was extracted on an element average basis. The estimated number of cycles to failure was then calculated using the Coffin-Manson fatigue model for the Sn3.5Ag solder [116]. An accumulated plastic strain of 0.048 over a thermal cycle was derived, corresponding to a fatigue life of 350 cycles.

The daisy chain resistances of all test assemblies monitored through 500 thermal cycles are plotted in Fig. 52(b). Predictably, the same trends reported for die-shear testing remain true for thermomechanical reliability. All daisy chains of ENEPIG assemblies failed after the first 200 cycles. The EP and EPAG-B finishes showed similar, though slightly improved, reliability. The highest reliability was achieved with the EPAG-A finish, with a decrease in assembly yield from 84.4% to 55.2% after 500 cycles. Shorter lifetimes than predicted by FEM were experienced. This can be explained by uncertainties and simplifications in modeling, including the non-consideration of intermetallics that practically increase interfacial stresses, as well as entrapment of fillers from the NCP material in the solder, introducing initial defects which degrade reliability.

(a)



	As-bonded yield
EP-A	82.8%
EP-B	90.6%
EPAG-A	84.4%
EPAG-B	73.4%
ENEPIG	73.4%

(b)

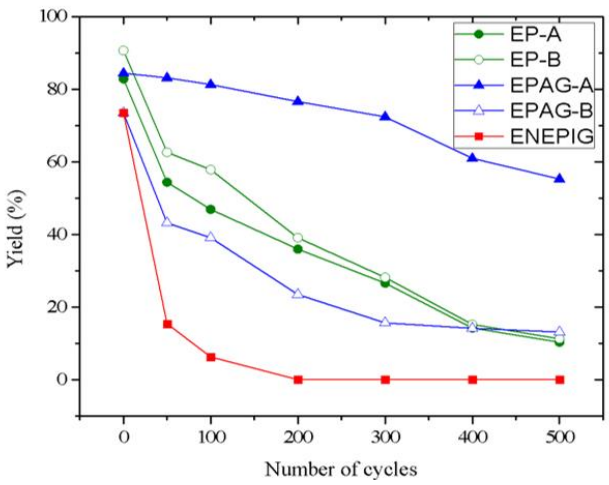


Figure 52. (a) The picture of assembled specimens and corresponding as-bonded yield, and (b) The electrical resistance monitored till 300 thermal shock cycles.

Based on die shear and thermal shock tests, it is clear that conventional ENEPIG surface finish can no longer meet reliability standards at fine pitch due to the increasing risk of (Au, Pd, Ni)Sn_4 precipitation. The new EPAG-A finish, composed of 50nm Au and 50nm Pd, has confirmed as the promising alternative for next generation off-chip interconnections. However, the structure of Cu microbump is required to modify accordingly, in which a reduced solder height less than 10μm and a Ni-free stackup are both necessary to stabilize the microstructure in case of serious Cu pad consumption or embrittlement. It's believed that the EPAGs would be adapted by the architecture with high density routings for demanding high-frequency performance. High as-bonded reliability over ENEPIG surface was confirmed in this section. However, the emerging needs driven

by other fields, such as power electronics, photonic packagings, and 3D-ICs, have brought even higher reliability requirements of thermal stability, power handling and even thermomechanical reliability. With EPAGs, a brittle conventional Cu-Sn SLID interconnection would be expected after extended HTS, and the maximum current density was still limited by unreacted solder. Therefore, the next task of this thesis is to design and demonstrate a new concept of metastable SLID bonding system, which is projected to satisfy the needs of pitch scalability, solder reduction, high thermal stability, and also high power handling capability.

4.4 Summary of intermetallics control with ultrathin surface finish

A new surface finish, electroless palladium autocatalytic gold (EPAG), was evaluated, at first with standard Cu pillar with 15μm SnAg and Ni diffusion barrier, and then with Ni-free ultrashort Cu pillar with 10μm SnAg. A comprehensive study, including characterization of solder wettability and interfacial reactions, as well as die shear and thermal shock tests, was carried out on EPAG and EP finishes to optimize their composition to achieve highly-reliable, fine-pitch, ultra-short Cu pillar assemblies. Standard ENEPIG finish was used as benchmark. Ideal solder wettability was achieved on EPAG and ENEPIG finishes, exceeding that on EP finish, which was found strongly dependent on the Pd thickness. Assemblies formed with optimal bonding conditions were subjected to 500h of high-temperature storage (HTS) at 150℃ to better understand interfacial reactions.

With standard Cu pillar, the connected joint was mainly composed of (Au, Ni, Pd)Sn_4, indicating an severe Au/Pd embrittlement issue. With EP-B and EP-C, the $PdSn_4$ precipitated on the substrate interface and stayed remained after 500h HTS. The early failure of thermal shock test found with ENEPIG, EP-B and EP-C corresponded those fragile bonded microstructure. With EPAGs, the as-bonded intermetallics were found sensitive to the composition of Au and Pd, but the microstructure gradually transformed into $(Cu, Au, Pd)_6Sn_5$ through HTS, regardless the compositions. A > 90% pass percentage was observed through 1000 thermal shock cycles with all EPAG compositions. In the phase II, the microstructure became more sensitive to the EP and EPAG compositions with ultrashort Cu pillars, having 10µm solder. In assemblies with EP and also EPAG-B finishes, $PdSn_4$ and Pd-rich (Pd, Au)Sn_4 phases were identified, respectively, indicating that Pd dominates the gold embrittlement mechanism with limited solder volume. In contrast, a unique interfacial reaction occurred with the EPAG-A finish, with formation of joints composed of a single intermetallic, $(Cu, Au, Pd)_6Sn_5$, successfully inhibiting gold embrittlement. The interconnection microstructure, resulting from the unique interfacial reactions between solder and surface finish, also controls the joints's strength and fatigue life, more so as the solder volume is reduced. The EPAG-A composition subsequently exhibited the highest die shear strength with a 40.5MPa average, and superior thermomechanical reliability, surviving over 300 thermal cycles with a thick organic package. The EPAG-A finish with 50nm Au and Pd thicknesses has thus been demonstrated as a promising low-cost alternative for highly-reliable, ultra-short Cu pillar interconnections, satisfying the design rule of 20µm pitch die-to-substrate interconnections.

CHAPTER 5. DESIGN OF METASTABLE SOLID-LIQUID INTERDIFFUSION BONDING

The proposed metastable SLID concept aims at extending pitch scalability of solder-based interconnections to below 20µm, and improving the thermal stability for 1000h at 200°C and power handling with 10^5 A/cm^2 current density. Though conventional SLID bonding technologies have been considered promising to satisfy those targets, this unique concept was designed to address the current challenges of standard SLID bonding technologies. To achieve this objective, it targets the intermediate Cu_6Sn_5 phase instead of the typical stable Cu_3Sn intermetallic, which yields lesser micro-voiding and volume shrinkage as well as accelerates reaction kinetics. The metastable SLID interconnection system was first designed from first principle based on theoretical kinetic and diffusion models, as well as thermomechanical modeling and electrical modeling for manufacturability, performance and reliability. Metastable SLID interconnections were then fabricated with the optimized stack-up, assembled and demonstrated at pitches down to 50µm, at this time. A reliability evaluation, including thermal stability, electromigration, and thermomechanical reliability tests, was finally carried out to fully demonstrate this technology.

5.1 Material design with thermodynamics and kinetics

The standard SLID interconnection system is composed of a Cu pillar, an ultra-thin intermetallic connecting layer and a Cu pad as described in Fig. 5(a). To stabilize the composition of the connecting layer to the metastable phase Cu_6Sn_5 without any further phase transformation into Cu_3Sn, the infinite Cu sources from Cu pillar and landing pad needs to be blocked off. This is achieved by introduction of Ni diffusion barrier layers, as

illustrated in Fig. 5(b). A diffusion couple composed of the semi-infinite Cu and 2μm Ni was first considered to evaluate the effectiveness of the barrier layer, ignoring the consumption of Cu from interfacial reactions happening in the real structure. Fundamental research on Ni/Cu interdiffusion was first conducted by Grube et al. [117], in which stable diffusivity of Cu through Ni, ranging from 0.91 to 1.2×10^{-14} m^2/s, was experimentally demonstrated at concentrations of 0.5-2.5wt%. The solution of Fick's law for interdiffusion between two pure metals, given by Equation 5, can be used in this study, assuming a constant diffusivity, with Cu concentrations lower than 1wt%:

$$\frac{C}{C_o} = 0.5 \times \left[2 - Erf\left(\frac{x}{2\sqrt{Dt}}\right) - Erf\left(\frac{-(x-2L)}{2\sqrt{Dt}}\right)\right] \quad (5)$$

where C is the Cu concentration in Ni, Co is the initial concentration, x is the distance from the interface used as origin, D is the diffusion coefficient, L is the thickness of the Ni layer, and t is the annealing time. Assuming the interdiffusion coefficients as in Cu-Ni thin films, using values published by Venos et al. [118], the diffusivity values for lattice diffusion and grain boundary diffusion at 250℃ were calculated as 2.66×10^{-25} m^2/s and 2.99×10^{-20} m^2/s, respectively. These numbers are slightly lower than those reported in other studies with higher annealing temperatures [117, 119]. These results indicate that annealing at 250℃ for 2800h would be required to increase the Cu concentration on top of Ni surface up to 1% of saturated concentration, suggesting that a 2μm Ni thickness is a sufficient diffusion barrier for Cu. However, deviations from the theoretical diffusion model are expected as electroless Ni(P) was used in this study instead of Ni. Unlike that of Ni, the microstructure of Ni(P) features nanocrystallines, expected with the standard phosphorus concentrations in electroless Ni plating bath of 7.6-9.84 at% [120, 121]. The effectiveness of Ni(P) as a

diffusion barrier was extensively studied and demonstrated by Sullivan et al. [122]. Consequently, 2µm-thick electroless Ni(P) layers were assumed as diffusion barriers to constrain the interfacial reaction.

The connecting layer, sandwiched by the Ni(P) barriers, was designed based on the following equation, used to define the thickness of the Cu and Sn layers:

$$\frac{t_{Cu}}{t_{Sn}} = \frac{6M_{Cu}/\rho_{Cu}}{5M_{Sn}/\rho_{Sn}} \quad (6)$$

where t is the thickness of the plated layer, M is the atomic weight and ρ is the elemental density. Considering, on one hand, the limitations of current electroplating processes in terms of height uniformity, and, on the other hand, the limited capability of SLID bumps to accommodate bump non-coplanarities, the symmetrical bump design of Fig. 53(a) consisting of 1µm-thick Cu and 2µm-thick Sn layers was defined to achieve the Cu_6Sn_5 exact composition and improve assembly yield. This approach was previously applied to design a multi-layered interconnection stack-up for conventional SLID bonding in the Cu-Sn system [123-125].

The transition time to achieve full phase transformation into Cu_6Sn_5 is another main key of manufacturability. A kinetic model was used to explain the growth mechanism of Cu_6Sn_5 and optimize the bonding thermal profile. Considering the symmetry of the interconnection design which involves two growth fronts, the transition time was determined based on the formation of Cu_6Sn_5 from consumption of 2µm of Sn and 1µm of Cu. The thickness of the resulting Cu_6Sn_5 layer can be calculated with the following equation:

$$\frac{t_{Cu}\rho_{Cu}}{6M_{Cu}} \times \frac{M_{Cu_6Sn_5}}{\rho_{Cu_6Sn_5}} = t_{Cu_6Sn_5} \quad (7)$$

where t is the thickness, M is the molar weight and ρ is the density. Based on equation (3), a 2.7μm-thick layer of Cu_6Sn_5 is expected to form from each growth front, giving a final thickness of the connecting layer of 5.4μm. This estimation is consistent with previous research on volume shrinkage from interfacial reaction. Further, the solid-liquid diffusion model established by Schaefer [126] enables the prediction of Cu-Sn intermetallic growth rates and was used to optimize the bonding conditions as follows:

$$X(t,T) = k_o \exp(\frac{\pm A}{RT}) t^n \quad (8)$$

where X is the average thickness of intermetallic, T is the temperature, and t is the reflow time. The three empirical parameters k_o, A and n are 17.5 μm/min$^{0.25}$, 9.0 kJ/mole and 0.25, respectively. Based on this solid-liquid diffusion model, full transition to Cu_6Sn_5 without any unreacted Sn can be achieved within 1min, which was used in bonding. A 20X reduction in bonding time was, therefore, predicted with the new approach, as compared to conventional SLID bonding strategies which typically require 20 to 30min to reach the ultimate Cu_3Sn stable phase.

The symmetrical bump design showed in Fig. 53(a) could be only adapted by 3D-ICs, but the cost and difficulties of plating multi-layered structure on the substrate limit the feasibility of being used for off-chip interconnections. Therefore, an asymmetrical bump design was modified for enabling the concept of metastable SLID to accommodate the standard ENIG or ENEPIG surface finish on the substrate, as showed in Fig. 53(b).

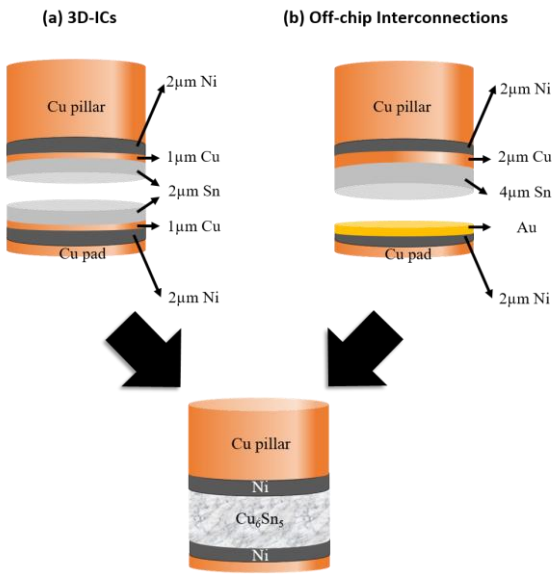


Figure 53. Schematic drawing of the metastable SLID with (a) symmetrical, and (b) asymmetrical bump design

5.2 Mechanical design for thermomechanical reliability

The main concern of thermomechanical reliability is the fatigue lifetime through the thermal cycling test, especially with the CTE-mismatched architecture and such short stand-off height. A FEM modeling was thus built to optimize the structure of metastable SLID bonding, benchmarking the standard Cu microbump but being scaled down to the same stand-off height. The 2D geometry was simulating the half diagonal of the assemblies, from the neutral axis to the corner. An assumption of plane strain condition was applied since the main deformation was expected to happen in in-plane direction. A total of 66 bumps was populated in this modeling with a bump diameter of 15µm at 30µm pitch. Fig. 54 shows the detailed geometry of this modeling, in which the standard Cu microbump was assumed to be bonded on the ENIG or ENEPIG surface finish, while the metastable SLID interconnect was composed of a 5µm-thick Cu_6Sn_5, sandwiched by the 2µm-thick Ni layer. A thick die of 550µm without backgrinding was introduced to fit the

real scenario in our lab, and a laminated 100μm-thick high CTE glass from Asahi Glass Corporation was used. The material properties were listed in Table 7 in Section 3.2, in which an Anand's viscoplastic model and a bilinear kinematic hardening model were used for Sn3.5Ag and electroplated copper, respectively. The cycling condition was set referring to the JEDEC TCT Standard - Condition B within the temperature range of -55℃ / 125℃ with a rate of 2 cycles per hour.

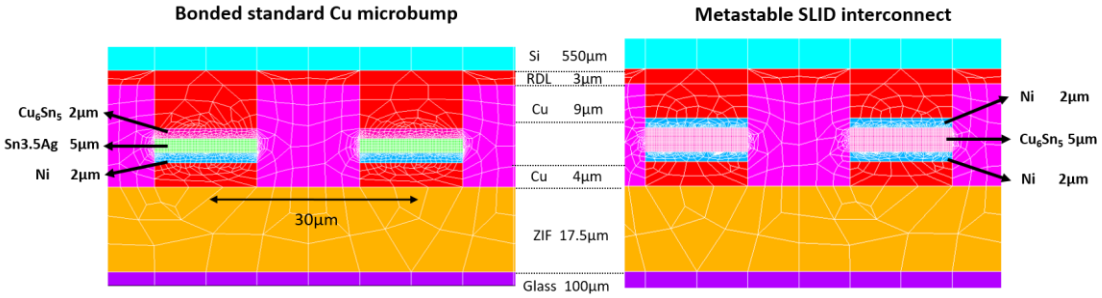


Figure 54. The FEM modeling of thermal fatigue lifetime estimation.

The results were extracted after the stress-strain curve had reached the steady state, and the maximum plastic strain was found at the bump farthest away from the neutral axis. An increment of plastic strain within solder showed a close value of 0.0857 through each thermal cycle, corresponding to a plastic strain amplitude of 0.0428. By applying the short lifetime fatigue Coffin-Manson Model, an estimated lifetime of 110-388 cycles were predicted, varied with the empirical parameters used [116, 127, 128]. This short estimated lifetime implies a serious thermomechanical risk of simply scaling the Cu microbump to reduced height for fine pitch without thoughtful design.

With the metastable SLID interconnection, the estimation can only be conducted based on a simplified stress-based approximation, since the modern fundamental understandings of fatigue are based on the plasticity of material deformation. The

intermetallics are believed to have more ceramic-like mechanical properties instead of that close to steel or copper alloy, and the established model or experiment focusing only on Cu_6Sn_5's fatigue behavior is not available to the best of our knowledge. As the modeling showed, an equivalent stress amplitude of 81 MPa was derived from the 3D stress amplitude through the thermal cycling. By applying the first-principle approximation, the metastable SLID joints composed of Cu_6Sn_5 were considered reliable due to the equivalent stress amplitude was significantly lower than Cu_6Sn_5's fatigue strength of 550MPa, which approximated to the half of its tensile strength. The experimental justification of thermomechanical reliability will be conducted in Section 7.4. Fig. 55(a) shows the accumulated plastic strain of solder in the case of standard Cu microbump, and Fig. 55(b) shows the first principal stress of Cu_6Sn_5 with metastable SLID interconnections.

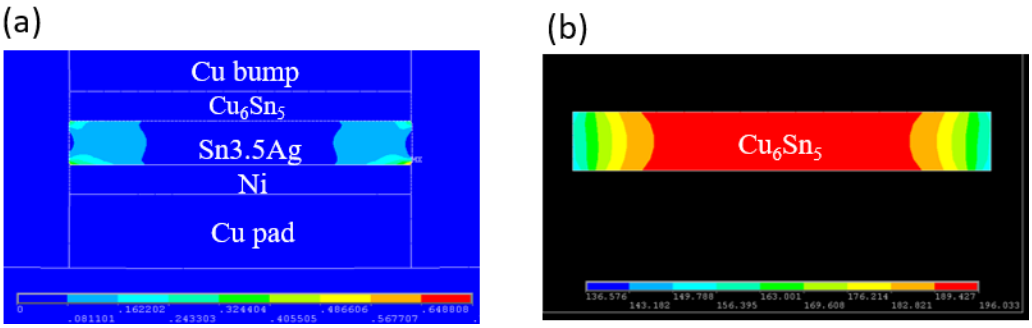


Figure 55. The FEM results of (a) accumulated plastic strain of solder with standard Cu microbump, and (b) 1st principal stress of Cu_6Sn_5 with metastable SLID interonncetions.

5.3 Electrical design for power handling capability and high performance

5.3.1 Electromigration evaluation

To achieve improved power handling capability beyond existing solder-based interconnection, the all-intermetallic interconnections have shown high potentials granted

by the lower diffusivities and higher modulus. This section provides the fundamental basis of using Cu_6Sn_5 in proposed structure. Since the electromigration behavior could be categorized into two types, substitutional diffusion and interstitial diffusion. It's necessary to consider both cases separately.

The concept of critical product is normally used for describing the self-diffusion process, in which the atoms are forced to move within the same type of matrix atoms accompanied with a counter-diffusion of vancancies, such as Al diffusion in the Al trace or Sn diffusion in the solder joints. A void gradually formed at the cathode interface and the resulting localized melt down are considered as the most common failure modes related to this self-diffusion process. Normally, the critical product derived from the balance between current stressing and backward mechanical stress can be used for estimating the threshold current density with a given migration distance. Equation 9 describes the critical product of electromigration [58]:

$$j\Delta x = \frac{\Delta\sigma\Omega}{z^*|e|\rho} \tag{9}$$

where j is the threshold current density, Δx is the migration distance, Δσ is the hydrostatic stress, Ω is the atomic volume, z^* is the effective charge, e is the charge of electron, ρ is the electrical resistivity. The Δσ could be considered proportional to the young's modulus of matrix material, and the radius of diffusant is corresponding to the Ω term. The effective charges (z*) referred to the literature [129]. Comparing the structure between a 10μm Cu-Cu interconnection, a Cu microbump with 15μm solder cap, and the designed metastable SLID with 5μm Cu_6Sn_5 connectied layer, the threshold current density for each is 1.8×10^6

A/cm^2, 10^4 A/cm^2 and 1.6×10^5 A/cm^2, respectively. A more than ten times improvement was predicted by replacing the Cu microbump with metastable SLID bonding, and the failure mechanism related to void propagation under current stressing thus could be efficiently prevented.

The interstitial diffusion relates to the dissolution of under bump metallization (UBM). The main difference is that the diffusants would not build the backward mechanical stress to balance the electron wind force, and a differential intermetallic growth rate can be observed between cathode and anode interface. The diffusion flux of those diffusant can be described as following Equation 10:

$$J = C\frac{D}{KT}Z^*|e|\rho j - D\frac{d\mu}{dx} \tag{10}$$

where C is the concentration of the element of interest, D is the diffusivity of atoms through the matrix, Z* is the effective charge number, ρ is the resistivity, j is the current density, e is the charge of electron and μ is the chemical potential. The driving force from electron flow is roughly two orders of magnitude higher than that from the concentration gradient. The overall diffusion flux is consequently dominated by electromigration. In solder interconnections, Cu atoms can easily be driven from the cathode to the anode through the solder which provides higher interstitial diffusivity of about 10^{-12} to 10^{-13} m^2/s at 25℃. The Cu atoms accumulated on the anode interface results in enormous intermetallic precipitation, and this diffusion flux keeps dissolving the Cu pads on the cathode interface to replenish the Cu concentration of solder. With Cu_6Sn_5, the diffusivities of 6.74×10^{-16} m^2/s for Cu and 5×10^{-18} m^2/s for Ni indicate a significantly reduced diffusion flux with all-

Cu_6Sn_5 joints. Under the same current density, a three to four orders of magnitude longer lifetime could be expected with metastable SLID interconnections than Cu microbumps.

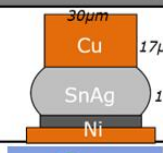
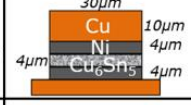
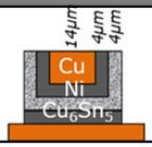
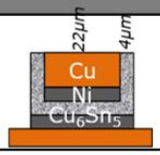
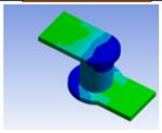
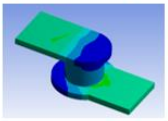
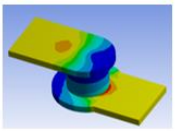
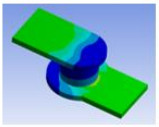
5.3.2 Design for high electrical performance

In order to control the interfacial reaction, the Ni diffusion barrier layer was introduced to interfere in the Cu source from bumps and pads. However, some electrical concerns have arose to challenging the usage of Ni for high performance electronics, due to its high electrical resistance. Even the Ni barrier layers have been widely adapted in current architectures for decades, including the Cu microbump and ENEPIG/ENPIG surface finishes, an evaluation of the compromised electrical performance followed by a proposed strategy to address this challenge is apparently necessary. A design modification thus was proceeded, based on the prerequisite multi-layered structure defined by aforementioned material and mechanical design. In this section, a direct-current (DC) electrical simulation will first be conducted with ANSYS Workbench to study the equivalent electrical resistance of different bump design. Secondly, an alternating current (AC) electrical simulation using the ANSYS High Frequency Electromagnetic Field Simulation (HFSS) will be conducted to evaluate the conductor loss up to 40 GHz. These modelings were completed with the technical support of GT-PRC graduate, Dr. Jialing Tong.

As showed in Table 10, three different metastable SLID bump structures, namely Structure A, B, and C, were designed to yield the same Cu_6Sn_5 intermetallics but with redistributed Ni and Sn layers. The standard Cu microbump with 17μm Cu bump and 15μm solder cap was used as the benchmark. All the bumps is designed with the same bump

diameter of 30μm. However, as the metastable SLID interconnections are projected for a reduced standoff height with mechanical reliability, the structure A, B, and C have a reduced Cu height of 10μm. A 300μm-long and 5μm-thick Cu trace was attached to the either end of the bump, enabling a uniform current excitation. By monitoring the DC voltage drops from one end of the interconnections to the other with a 0.2 A current excitation, the equivalent electrical resistances of different bump structures could be estimated. As summarized in Table 10, the initial design of Structure A, which has the lowest resistance, achieves a 0.3 mΩ resistance reduction, compared to the standard Cu microbumps. The structure B has the highest resistance due to its minimum copper area in the cross-sectioned plane. The DC modeling shows a promising result of metastable SLID interconnections that brings a similar resistance range of current standard Cu microbumps, without jeopardizing the established electrical design guidelines.

Table 10. The equivalent electrical resistance and corresponding current density distribution of different bump structures.

	Standard Cu Microbump	Structure A	Structure B	Structure C
				
Current density distribution				
Nominal electrical resistance	R=9.69mΩ	R=9.31mΩ	R=10.41mΩ	R=9.90mΩ

Then, the high-frequency performances of Structure A, B, and C were compared to the standard Cu microbump and Cu-Cu interconnections. To ensure the current loop, a pair of interconnections were designed at the minimum pitch for each structure with one signal interconnection and one ground interconnect, as shown in Fig. 56(a). The surrounding environment was set to be vacuum to eliminate the dielectric loss. The simulated conductor losses for different structures are presented in Fig. 56(b). It is found that the Cu-Cu interconnections have the lowest conductor loss thanks to the exceptional conductivity of copper. Even though the Structure A shows lowest DC resistance in the previous DC model, it has the highest conductor loss in this AC model, which is attributed to the low conductivity of Ni and the skin effect. The Structure B and C shows almost identical performance to standard Cu microbump. According to results of DC and AC modelings, the structure C was considered as the optimal structure having almost identical electrical performance to Cu microbumps. In the Section 6.2, a bumping process of Structure C will be described, using the electroless platings. Since both Structure C and A were expected to

have same interfacial reaction and corresponds to our unique approach, the initial design, Structure A, will still be used for the assembly and reliability demonstration in this study.

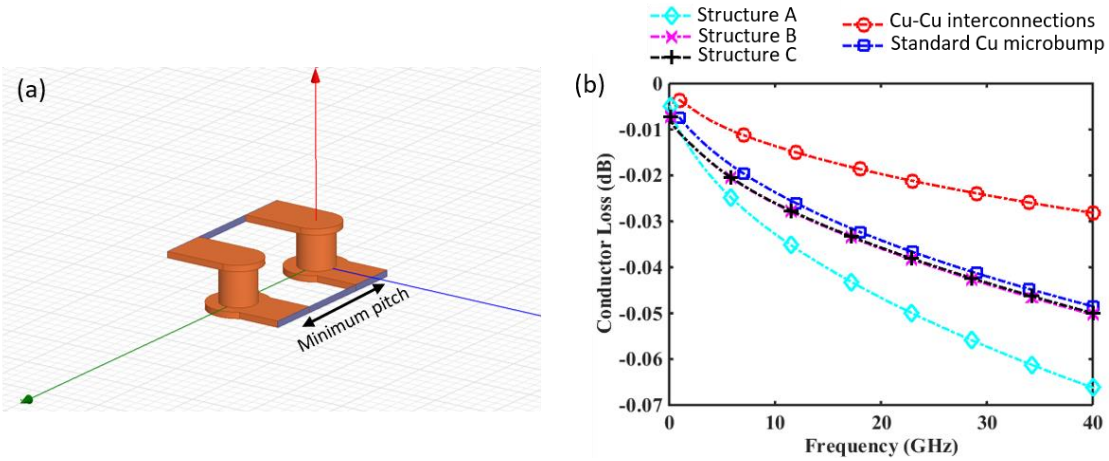


Figure 56. (a) The geometry of ANSYS-HFSS model, and the (b) chart showing the conductor loss vs. frequency with different bump structures.

CHAPTER 6. BUMPING AND ASSEMBLY OF METASTABLE SOLID-LIQUID INTERCONNECTION BONDING

To enable the designed structure as mentioned in Chapter 5, this chapter will first focus on the bumping process developed for multilayered plating with accurate thickness control. The section 6.1 will describe the electrolytic plating process to achieve the initial bump structure, as labeled as Structure A in Table 10. The novel development of electroless bumping process will the first time demonstrate in the section 6.2, to enable the customized bump structure of Structure C. In the third section, the fabricated metastable SLID bumps will then be assembled on Si and ultra-thin glass substrates through TC-NCP process.

6.1 Bumping with electrolytic plating

A two-step photo-lithography process was used for wafer fabrication, following the process flow presented in Fig. 57. The 15μm-thick Hitachi RY-5315EB dry-film photoresist and 25μm-thick Hitachi Sample A dry-film were used for patterning of the routing and bump layers, respectively. Development was performed with a 3% Na_2CO_3 solution at 85°C, followed by plasma etching to remove the residual organics that could contaminate the opened area. The Cupracid TP and Sulfotech-LST chemistries were used for copper and tin electrolytic plating, and the Ni(P) barrier layer was plated with the electroless Aurotech CNN chemical. A current density of 2 ASD was first used for Cu deposition to form the routing and bump layers. After Ni(P) electroless plating, lower plating rates of 0.75 ASD and 1ASD were used for copper and tin plating, respectively, in order to control the plated thickness more accurately. Through the whole process, the thickness could be well-controlled via the dipping or plating time. The Enthone PC 4025

stripper solution was then used to strip the photoresist, and the Cu/Ti seed layer was etched by Transcene Copper Etchant 49-1 and HF.

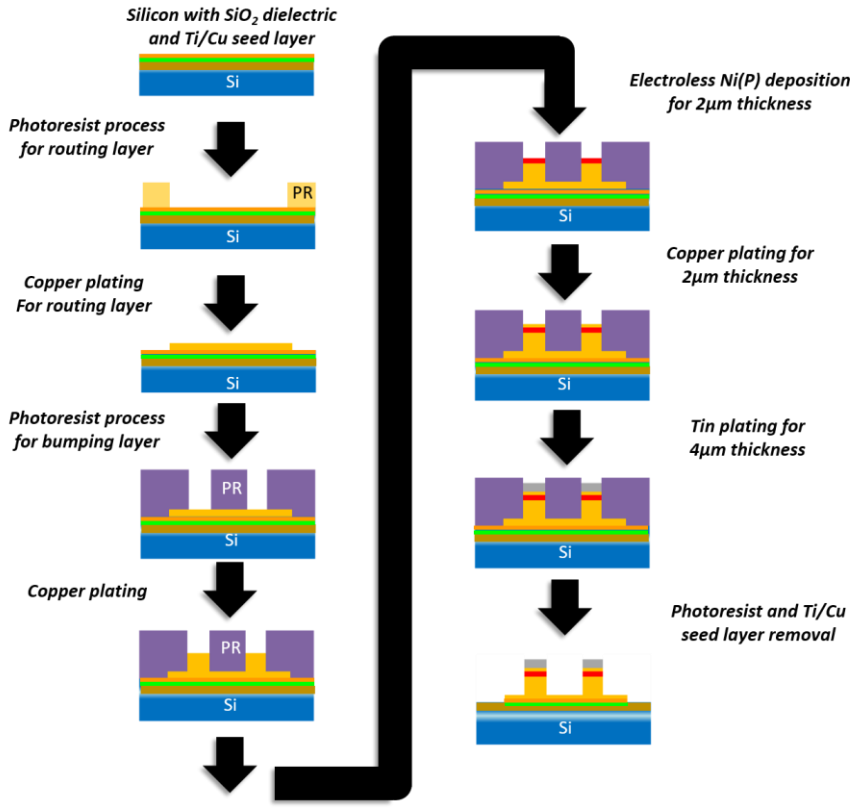


Figure 57. The bumping process flow of metastable SLID using electrolytic plating.

The fabricated bump is showed in Fig. 58. The averaged thickness of Cu, Sn, and Ni(P) was 1.8µm, 3.9µm and 1.7µm, respectively. The thin Au layer observed was designed as the adhesion layer between Ni(P) and Cu, and was not expected to affect the wanted interfacial reaction. To evaluate the manufacturability of bumping this alternating Cu/Sn structure, a uniformity and repeatability plating test was conducted with three 6-inch wafers, 10 samplings with 3 trials for each. The total variation (TV) was found as 0.26µm, ignoring the appraiser variation (AV). From the design point of view, based on the Cu-Ni-Sn ternary phase diagram [130], the targeted phase of $(Cu, Ni)_6Sn_5$ has a wide composition

range from 21.4 at% to 54.5 at% of Cu, benefited from the substitution of Ni for Cu. This wide composition range reflects an acceptable plating tolerance of 1.23μm, which is five times larger than the total variation measured from the uniformity and repeatability test. An outstanding manufacturability was thus confirmed with metastable SLID bumps. For designing the metastable SLID bonding, the case of excessive Sn atoms is preferred than that of excessive Cu atoms, since the insufficient Cu atoms to form Cu_6Sn_5 could still be replenished by Ni substitution. In the opposite case of excessive Cu atoms, the phase of Cu_3Sn was expected to form as that in the conventional Cu-Sn SLID bonding, and some voids caused by phase transformation were expected.

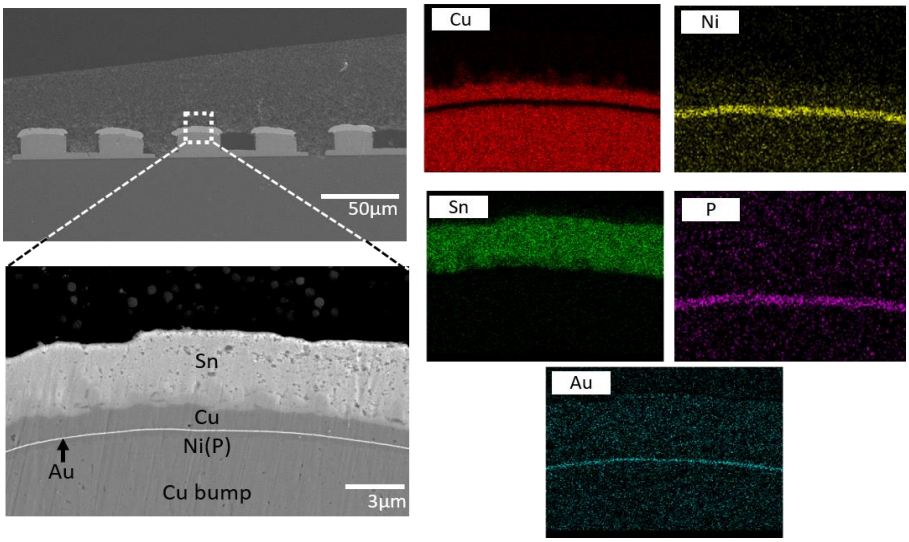


Figure 58. SEM image of plated bumps, and the high-magnification view of the multilayered stack and corresponding XEDS mapping.

6.2 Bumping with high-speed electroless process

Metastable SLID bonding relies on a multilayered bump structure consisting of 2μm Ni, 2μm Cu and 4μm Sn and requires a precise control of thickness and composition.

Even though a low total variation was successfully achieved with electrolytic plating process, the high uniformity would be challenged if using common plating rate in manufacturing. Considering electrolytic plating tolerances at larger wafer scale, bumping manufacturability is a clear challenge that needs to be addressed. Electroless processes enable better control over thickness and uniformity. In addition, in order to fabricate the customized bump structure, namely Structure C in Table 10, the electroless process indeed shows higher flexibility of bumping. However, current electroless processes are typically targeting very thin layers with much lower deposition rates than electrolytic processes. With the trade-off between precise thickness control and deposition rate, the potential solutions can be either the electrolytic plating with low current density or the special electroless plating with high deposition rate. In this section, the applicability and potential of electroless process for high-precision wafer bumping were explored.

To replace electrolytic plated Sn with electroless Sn, a commercial immersion tin chemicals were used to modify the properties for our special application, and especially evaluate the sacrificed Cu layer thickness to be replaced by immersion Sn. Immersion tin plating using the Stannatech 2000V chemistry from Atotech GmbH was set up and applied on a thick Cu-clad FR-4 substrate with an 18µm Cu thickness. The plated Sn surface formed after 200min of deposition was observed by SEM/XEDS. A thickness of 4.4±1.2µm was achieved with a scalloped Sn morphology as shown in Fig. 59(a). Furthermore, the Ag atoms from the anti-whisker additives were detected in the Sn layer, which could potentially affect the targeted interfacial reaction. The plating trials were consequently repeated without additives, with the results of Fig. 59(b). With the same deposition time, the Sn layer presented this time a planar surface with a slightly higher

thickness of 4.65±0.86µm. The consumed Cu thickness was also defined as 5-6µm. The Sn layer optimized with immersion tin process will then be implemented into the bumping process.

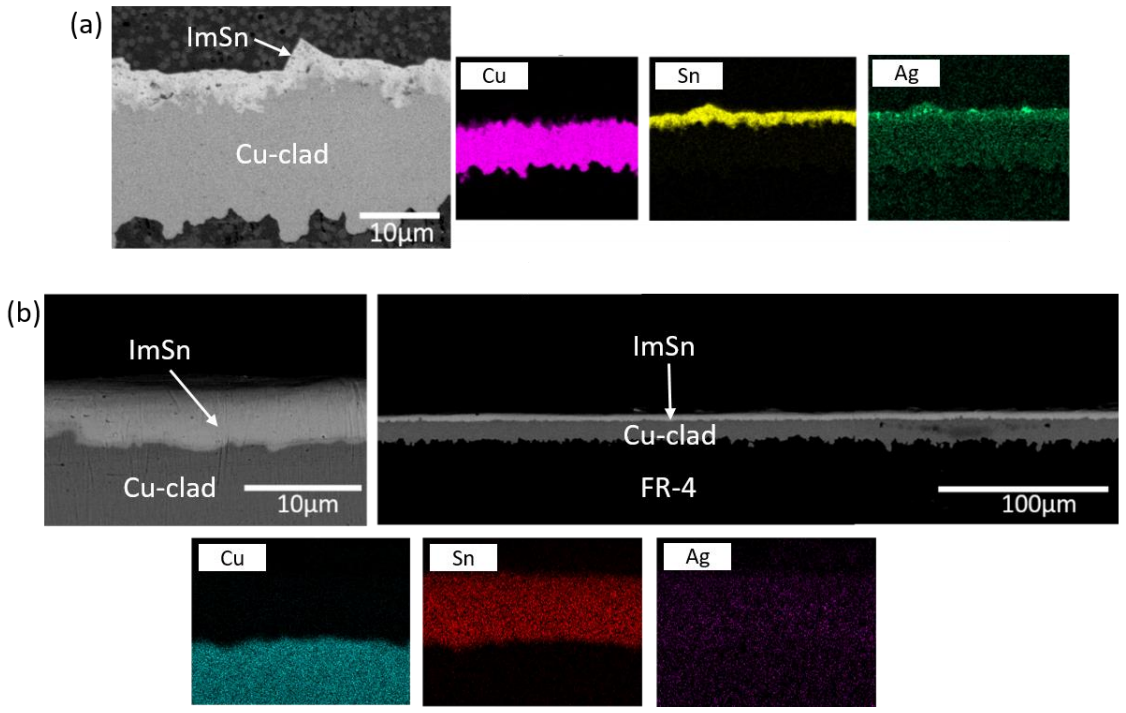


Figure 59. The immersion Sn deposition on Cu-clad FR-4 (a) with, and (b) without anti-whisker additives.

Based on the design optimization for high frequency performance and low resistance, a core-shell bump of Structure C is the optimal configuration. The bumping process was defined as Fig. 60(a). The main improvement was a SiNx was deposited as a passivation for preventing the delamination caused by subsequent electroless bath. The first proof-of-concept was showed in Fig. 60(b). The focused-ion-beam (FIB) cross-section showed a clear structure with a core of Ni(P)/Cu stackup and a shell of immersion Sn, as designed. However, the thickness of Ni(P), Cu and Sn, measured as 1.2µm, 3.9µm and 1.9µm, were deviated from the designed structure. A co-development with Advanced

Seimiconductor Engineering (ASE), Atotech GmbH with improved process control was then proceeded with a memory wafer resourced from Global Foundries.

The simplified process flow was showed in Fig. 61(a), in which the core bump structure was electrolytically plated by ASE with a 8μm-thick Cu bump, a 4μm-thick Ni barrier and a 2μm-thick Cu. After the photoresist and seed layer removal, the wafer was then deposited with a high speed electroless Cu with a target thickness of 5-6μm in Atotech GmbH, defined by the previous trials with Cu-clad FR-4 test boards for following immersion Sn process. A Cu shell with ideal coverage was achieved, as showed in Fig. 61(b). The immersion Sn process was then again proceeded in GT-PRC for exchanging the electroless Cu shell with immersion Sn. The fabricated bump of the Structure C is showing in Fig. 61(c), with an improved thickness control of each layer than previous batch. However, an overactive corrosion was happening through the immersion Sn process because of the columnar morphology of high speed electroless Cu. This challenge could be partially improved by condensing the electroless Cu by high temperature annealing, but the compatibility between high speed electroless Cu and immersion Sn apparently needs to be addressed to completely derive this bumping process.

In this section, the bumping process with electroless Cu and immersion Sn shows a promising alternative to achieve improved uniformity and highly customized bump structure. Even though the designed process flow is premature and bringing challenges to foundries and chemical suppliers, the study has pointed out a new concept of bumping process for next phase and the first time demonstrated it as the proof-of-concept.

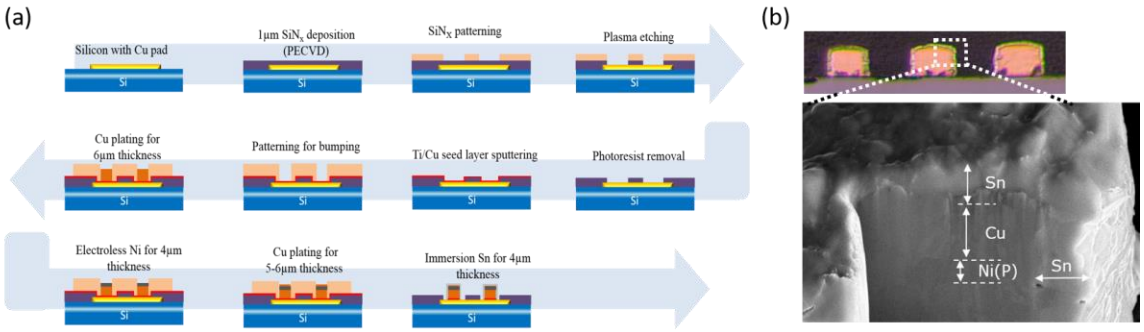


Figure 60. The (a) process flow, and (b) FIB cross-section of the fabricated bump through electroless bumping process in the first trial.

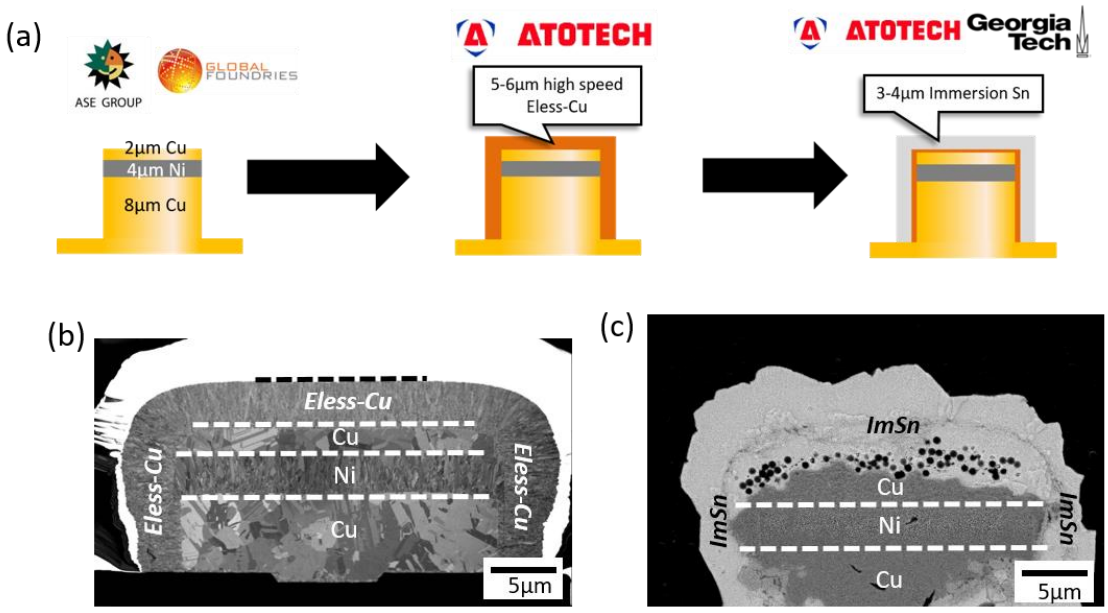


Figure 61. (a) The process flow of co-development of electroless bumping with industry partners, and the SEM image of the bump after (b) high speed electroless Cu, and (c) immersion Sn.

6.3 Assembly of metastable SLID bonding with architectures of 3D-ICs and off-chip interconnections

This section describes the assembly processes and resulting microstructure of first the symmetric metastable SLID architecture on a 650μm-thick Si substrate, then the

asymmetric architecture on a 100µm-thick laminated glass substrate. The technology was projected to both 3D-ICs and off-chip interconnection applications, as described in Fig. 53.

6.3.1 Assembly of symmetric structure for 3D-ICs

A lab-scale Finetech Fineplacer Matrix flip-chip bonder was used for assembly in this section. The demonstration of metastable SLID bonding for 3D-ICs configuration was successfully achieved with TV1 on a 650µm-thick silicon substrates. The assemblies were formed by thermocompression bonding but with the heat from both die and substrate side to mimic the reflow process of 3D-IC stacks. The peak temperature was set as 260℃, and a pressure of 40MPa was applied to compensate the non-coplanarities of the bumps. As showed in Fig. 62, the void-free interconnections composed exclusively of $(Cu, Ni)_6Sn_5$ were achieved with only 1 min dwell time at peak temperature as predicted by Equation 8. A 20X reduction in bonding time was, therefore, achieved with the new approach, as compared to conventional SLID bonding strategies which typically require 20 to 30min to reach the ultimate Cu_3Sn stable phase. Theoretically, 2.7µm-thick layer of Cu_6Sn_5 is expected to form from each growth front by consuming 2µm of Sn and 1µm of Cu, indicating a final thickness of connected layer of 5.4µm. The $(Cu, Ni)_6Sn_5$ thickness from this study ranged from 3.4-4.5µm could be contributed by the solder collapse through the assembly process.

In order to further improve the assembly throughput, the dwell time at peak temperature was shorten to 30s. As showed in Fig. 63(a), the phase transformation into $(Cu, Ni)_6Sn_5$ was not completed and some unreacted Sn remained. In addition, a crack was found propagating through the interface between $(Cu, Ni)_6Sn_5$ and remained solder. In

conventional solder microbumps, relatively large volume of solder acts as the role of providing compliance for entire interconnections. While the solder volume is extremely limited as the scenario observed in this study, the energy introduced by CTE-mismatched between chip and substrate cannot be completely absorbed by the solder plasticity. As the result, a built-up stress concentration located at the heterogeneous interface of intermetallics and solder eventually tear the interconnections, during the assembly cool-down phase. A two-staged assembly process was then proposed to address this fundamental challenges, which was composed of a similar thermocompression bonding process but with only 3s dwell time and a subsequent standard reflow cycle. The concept was to initiate the metallurgical bonding through the thermocompression bonding within a short dwell time, in which the growing $(Cu, Ni)_6Sn_5$ was expected to be less than 1μm and the majority of the connecting layer would be still contributed by solder, providing the required compliance to survive the cool-down phase of thermocompression bonding. The full transition to target intermetallics would then be completed through the following one reflow cycle, which could be integrated into the board-level SMT (Surface Mount Technology) process. The single-phase connected layer was demonstrated with this two-staged assembly process, as showed in Fig. 63(b), providing a compelling SLID technology compatible to current industry-standard assembly process with high throughput.

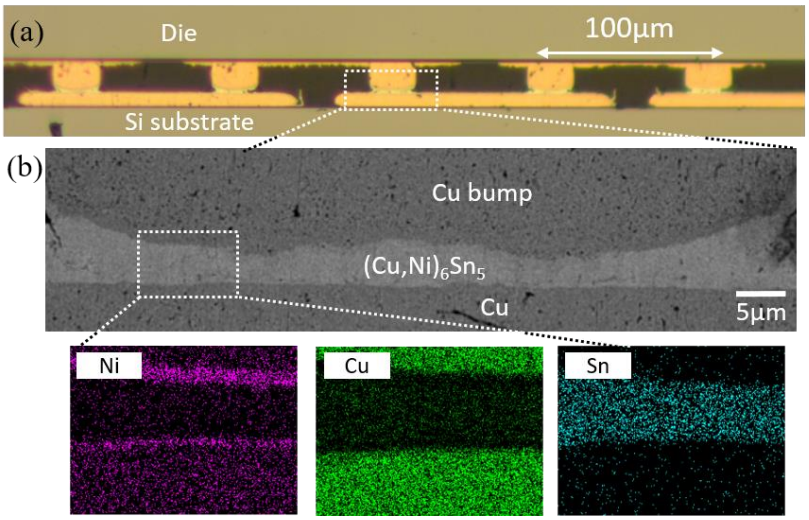


Figure 62. The (a) optical image, (b) SEM images and XEDS-mapping of assembled metastable SLID bonding.

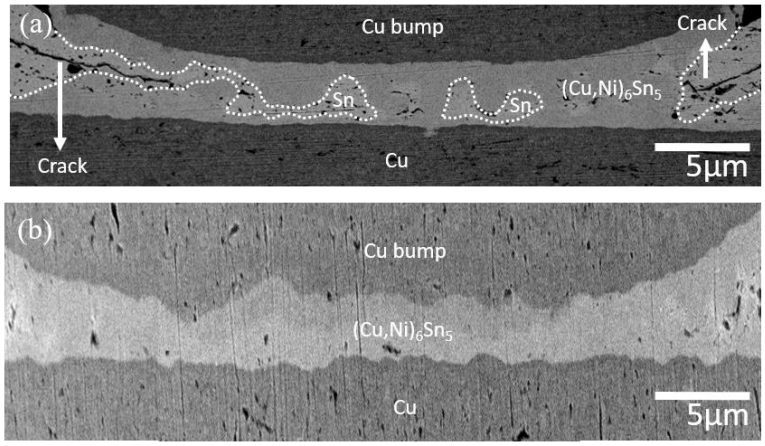


Figure 63. The cross-sections through (a) thermocompression bonding with 30s dwell time and (b) two-staged assembly process.

6.3.2 Assembly of asymmetric structure of off-chip interconnections

One of the main challenges of accommodating the metastable SLID bonding technology to chip-to-package configuration is to optimizing the optimal ENIG surface finish, having ideal solder wettability and meanwhile avoiding the Au embrittlement caused by $AuSn_4$. With standard Cu microbump, limiting the Au concentration within

solder less than 0.1wt% used to be the design guideline of preventing Au embrittlement in the past decades. However, accompanied with the scaling, the reduced solder height dramatically increases the Au concentration in solder. It has been reported recently [110], the Au embrittlement no longer can be avoided simply by reducing the Au thickness in ENIG surface. In our structure, the conventional 17-25μm-thick solder was significantly reduced to 4μm-thick, corresponding to a 6.2wt% Au concentration given a 100nm-thick Au. To preventing the Au embrittlement, a study of metastable SLID bonding on ENIG surface finish with varying Au thickness, ranged from 50nm to 150nm was conducted. The cross-sections of the as-bonded assemblies were showed in Fig. 64, in which the $AuSn_4$ was not observed in the cases of 50nm and 100nm-thick Au. This finding could be well explained by the Cu-Sn-Au ternary phase diagram, which indicates the $(Cu, Au)_6Sn_5$ high temperature phase (η) having a complete solid solubility with (Au, Cu)Sn [131]. Through the assembly, the Au atoms were first dissolved into the melt solder, and the phase equilibrium shifted toward to the two-phase region of $(Cu, Au)_6Sn_5$ and Sn, preventing the precipitation of $AuSn_4$. Another finding is that, with an Au thickness of 150nm, the $(Cu, Ni, Au)_6Sn_5$ growth rate was significantly reduced and an excessive amount of unreacted Cu remained, as showed in Fig. 64(c). More fundamental studies are still required to fully understand this phenomena, but the higher Au concentration in $(Cu, Ni, Au)_6Sn_5$ is likely requiring an extended diffusion time to rearrange the substitutional lattice site of Cu, Ni and Au. In addition, a high concentration of Au and $AuSn_4$ precipitates in the remained solder right front of the $(Cu, Ni, Au)_6Sn_5$'s growth front are also expected to pin the proceeding movement of the interface. With the interest of assembly throughput and prevention of gold embrittlement, ENIG surface with less 100nm-thick Au layer is thus

suggested. However, an ultrathin Au layer was widely acknowledged as porous, which deteriorates the solder wettability due to the strong inclination of Ni oxidation [132]. The ENIG surface with 100nm-thick Au layer was thus selected as the optimal surface for metastable SLID bonding and applied to all the substrates demonstrated in this study.

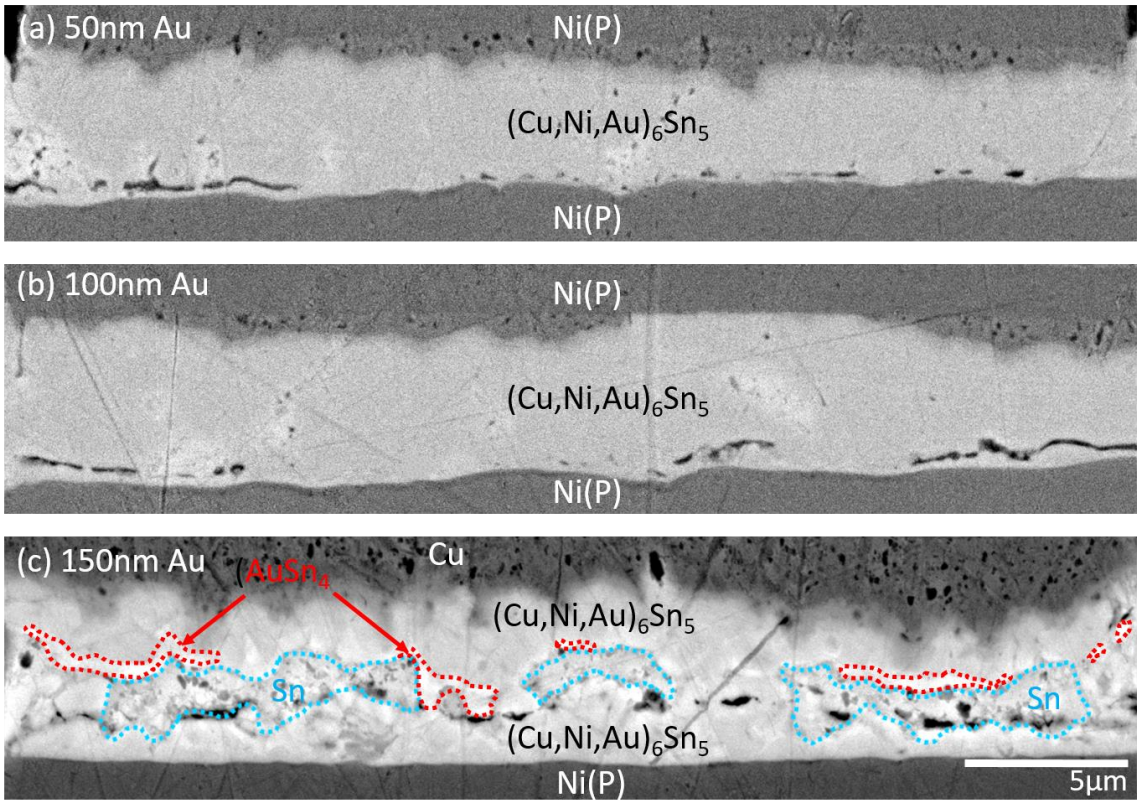


Figure 64. The cross-sections of the assemblies on ENIG surface with (a) 50nm (b) 100nm, and (c) 150nm-thick Au.

A 100μm-thick laminated glass substrate was then fabricated, following the process described in Section 3.1.2 with optimized ENIG surface finish. As described in Section 3.2, the major difference of TC-NCP from mass reflow is having a temperature gradient built up through the package, in which the stage temperature was normally set as 70℃, constrained by the thermal stability of pre-applied underfill materials. In order to reach the

melt point of solder, higher peak temperature than that of mass reflow is required to apply on the tool head, and this critical parameter was found highly sensitive to the package architecture. Fig. 65 shows the cross-section of the first assembly trial, in which a tool head peak temperature of 400℃ was applied for 1min. However, the full transition to (Cu, $Ni)_6Sn_5$ was not completed and some excessive Cu was found remained on the bump interface. This result implied that the actual peak temperature of the solder was lower than the target temperature of 260℃. Since the design of phase transformation was based on the reacting temperature at 260℃, and the interdiffusion rate is ruled by the Arrhenius equation, an interconnection composed exclusively of (Cu, $Ni)_6Sn_5$ thus could not be achieved. Referred to the thermal modeling and experimental justification did in Section 3.2, the temperature in the solder was predicted as 244℃ with a peak tool head temperature of 400℃, just exceeded its melting point. A higher peak tool head temperature was indeed required to demonstrate the full transition at 260℃ bonding temperature, as designed. However, being limited by the maximum tool head temperature available with lab-scale flip-chip bonder, the target off-chip interconnections temperature of 260℃ could not be achieved with the 100μm-thick glass substrate. As alternative, the modified assembly dwell time was corrected based on Equation 8 to correspond to the actual bonding temperature of 244℃. As showed in Fig. 66, the metastable SLID interconnections was then achieved with an extended 1min 30s dwell time. The minor pockets of residual solder were likely caused by the impingement effect of the intermetallics growing from both interfaces, in which the growth rate was slowed down after the (Cu, $Ni)_6Sn_5$ grain being hindered by the counter-growing grain. Those small pockets of residual solder were not expected to affect the overall reliability.

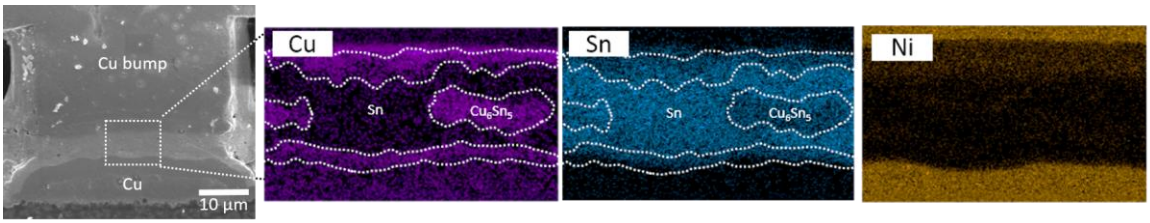


Figure 65. The incomplete phase transition with 100µm-thick glass substrate through TC-NCP, having 400℃ tool head temperature and 70℃ stage temperature for 1min dwell time.

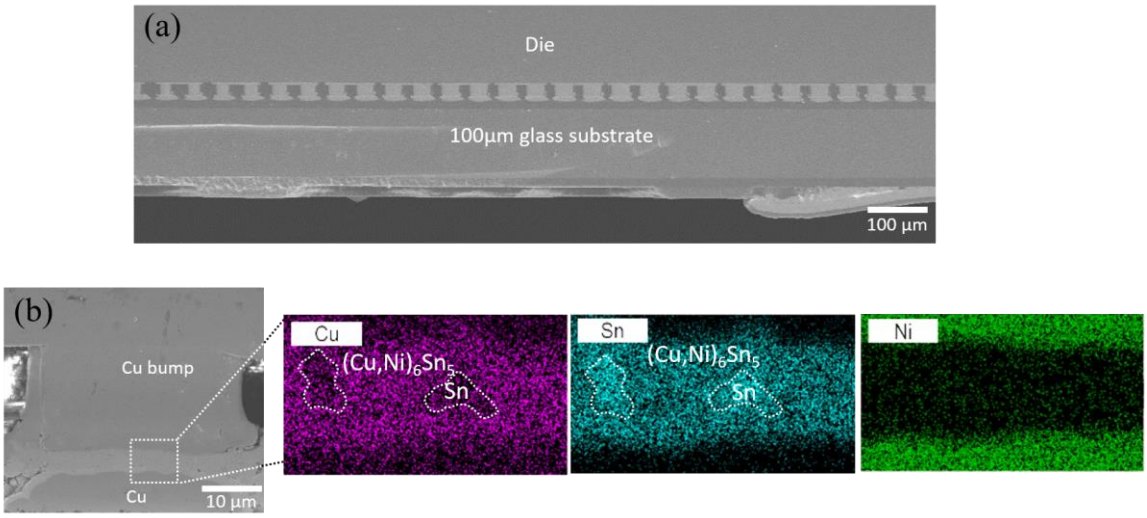


Figure 66. Assemblies of full transition with 100µm-thick glass substrate through TC-NCP process, having 400℃ tool head temperature and 70℃ stage temperature for 1min 30s dwell time.

In this section, the metastable SLID interconnections were demonstrated with the architectures of both 3D-ICs and off-chip interconnections. The full transition to target $(Cu, Ni)_6Sn_5$ was successfully achieved within 1min bonding dwell time at 260℃, as predicted from the theory. The design can further be accommodated with manufacturing TC-NCP and SMT process through a delicate control of interfacial reaction. The assemblies will then be subjected to reliability tests in the next chapter.

CHAPTER 7. RELIABILITY AND CHARACTERIZATION OF METASTABLE SOLID-LIQUID INTERDIFFUSION BONDING

In this chapter, the reliability of metastable SLID bonding will be experimentally evaluated based on the objectives defined at the beginning of this thesis. A die shear test will be conducted for as-bonded strength, and the thermal stability will be tested through multiple reflow test and high temperature storage up to 1000h at 200℃. The superior power handling capability will be showed with an electromigration test at 10^5 A/cm^2 current density. The ultra-thin glass package using metastable SLID bonding will then be subjected to thermomechanical reliability test. Founded on all the learnings built up in this thesis, the 20µm-pitch metastable SLID interconnection will be finally demonstrated in the end of this chapter.

7.1 Die shear test

Daisy-chain samples of TV1 design were assembled without pre-applied underfill to quantify the quality of the joints through die-shear testing. The assemblies were formed by 1min thermocompression bonding at 260℃ with an applied pressure of 10MPa to compensate for bumps non-coplanarities. Die-shear test was carried out following the MIL-STD-883G Method 2019.7, which is used for bonding strength evaluation of die-attach technologies. For a die size of 25mm^2, the minimum force required to pass this standard is of 2.5 kgf, or 6MPa with considerations of the total bonded area that actually contributes to the overall strength. A Dage-Series-400 bond tester was used for this evaluation, with a die-shear cartridge of 10 kgf. The speed of the shear tool was set to 32.0µm/s, and the tool

height was 5µm which was defined as the distance from the tip of the contact tool to the top of the substrate. Shear strength values in MPa were derived from the maximal loading measured (kgf) before failure.

Shear testing was carried out on 10 samples assembled in ideal conditions to qualify the bonding strength of metastable SLID interconnections. The measured shear strengths varied from 76MPa to 97MPa with an average strength of 88MPa, more than 10X the minimum MIL-standard. A bonding strength averaging 40MPa has been reported for state-of-the-art Cu-Sn SLID bonding, limited by crack propagation through the Cu_6Sn_5/Cu_3Sn interfaces or within the Cu_3Sn layer due to Kirkendall voids [125, 126]. In the case of metastable SLID bonding, brittle fracture happened through the bulk of the void-free Cu_6Sn_5 layer. This was confirmed by observation of the fracture surfaces shown in Fig. 67 in which Cu_6Sn_5 was found on both sides of the fracture interface. The high fracture strength of Cu_6Sn_5 contributed to the enhanced bonding strength of metastable SLID interconnections. No Cu_3Sn or Ni/Cu layers were observed on the fracture surface by XEDS analysis, which further indicates that the designed barrier layers can successfully inhibit the growth of Cu_3Sn. No adhesion issues between the stacked layers were either observed.

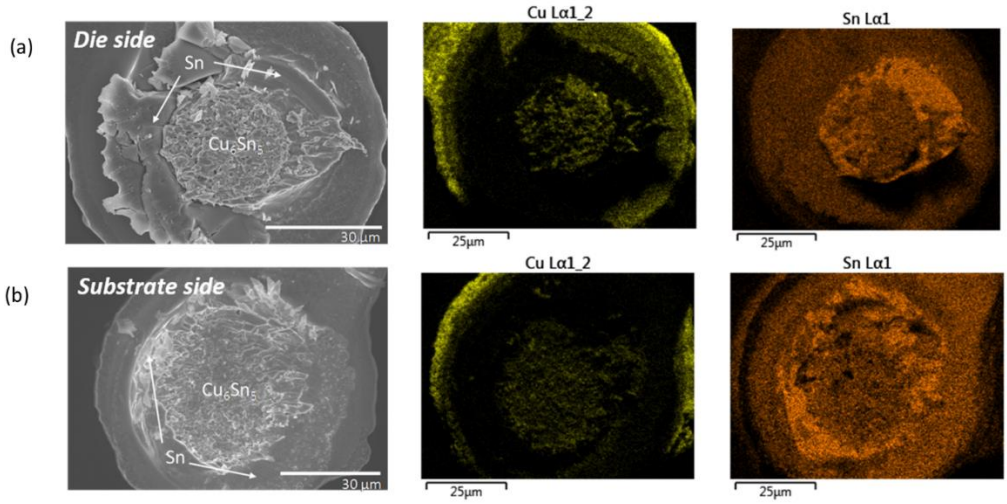


Figure 67. SEM images and corresponding XEDS mappings of the sheared surfaces on (a) die side and (b) substrate side.

7.2 Thermal stability test

Simple daisy chain TV1 at 100µm pitch were used for an evaluation of the thermal stability of metastable SLID interconnections. A test through 10X standard reflow cycles was first conducted, and the daisy chain resistances were measured after each reflow cycle with 22 out of 24 daisy chains surviving this multiple reflow test with steady electrical resistances, as seen in Fig. 68(a) and (b). The cross-section of an assembly after 10X reflow is shown in Fig. 68(c) and (d). The Ni(P) barrier layers remained intact even after multiple reflows and the intermetallics forming the connecting layer were confirmed as $(Cu_{0.94}Ni_{0.06})_6Sn_5$ by XEDS mapping and point analysis indicating 3at% of Ni substitution. The microstructure evolution was further studied through high temperature storage (HTS) at 200℃ up to 1000h. Fig. 69 shows the semi-in situ BEI images of the same cross-sectioned connected interconnect, and the zoom-in image and corresponding XEDS mappings after 1000h HTS are showed in Fig. 70. As predicted, the metastable SLID interconnections were found still composed of $(Cu_{0.63}Ni_{0.37})_6Sn_5$ without further phase

transformation into Ni-rich phases, implying a superior thermal stability under high operating temperature. The increased Ni substitution of Cu lattice site than that after 10X standard reflow cycles were expected, since a HTS at 200℃ with such extended aging time was considered as a severe thermal stability test, apparently beyond the capability of conventional solder-based interconnection technologies.

During thermocompression bonding, the diffusion path may pass through the Sn + $(Cu_{1-x}Ni_x)_6Sn_5$ two-phase region with minimum involvement of Ni, then reach the $(Cu_{1-x}Ni_x)_6Sn_5$ single-phase region. At this point of the process, the Ni concentration in Cu_6Sn_5 was under the detection limit of XEDS. After full transition into intermetallics, Cu_6Sn_5 is sandwiched by Ni(P) barrier layers, in which the diffusion path is then turned toward the Sn + $(Cu_{1-x}Ni_x)_6Sn_5$ + $(Ni_{1-x}Cu_x)_3Sn_4$ three-phase region since the ratio of Cu and Sn is now fixed. The Sn-Cu-Ni ternary phase diagram indicates that Cu_6Sn_5 can accommodate 32 at% of Ni substitution in the form of $(Cu_{0.41}Ni_{0.59})_6Sn_5$ [135]. Formation of $(Cu_{1-x}Ni_x)_6Sn_5$ has also been experimentally confirmed, including the study of Ni doping in solder [41] and of the Cu/solder/Ni diffusion couple [136]. Addition of Ni into solder was demonstrated to further stabilize $(Cu_{1-x}Ni_x)_6Sn_5$ and accelerate the growth rate of $(Cu_{1-x}Ni_x)_6Sn_5$ [42]. This would degrade thermomechanical reliability of traditional Cu pillar interconnections due to massive intermetallic formation, but is beneficial here by increasing the intermetallic transition rate, hence the assembly throughput. Formation of Cu_6Sn_5 during thermocompression bonding can be simplified as the reaction between Cu and Sn without involving Ni since molten solder is not in direct contact with the Ni layers in the symmetrical design. During the multiple reflow test or HTS, the Ni/Cu_6Sn_5/Ni diffusion

couple this time plays a key role, and is a determining factor in the outstanding thermal stability of metastable SLID interconnections.

Dissolution of Ni into solid Cu_6Sn_5 is mainly dominated by the diffusivity of Ni through Cu_6Sn_5. Though a Ni/$(Cu_{1-x}Ni_x)_6Sn_5$/Ni composition was identified after assembly, consistently with previous Ni-Sn studies with massive Cu concentrations [137], a very thin $(Ni_{1-x},Cu_x)_3Sn_4$ layer is necessarily formed between Ni and $(Cu_{1-x}Ni_x)_6Sn_5$ to respect thermodynamic equilibrium. The Ni concentration at the interface between $(Ni_{1-x},Cu_x)_3Sn_4$ and $(Cu_{1-x}Ni_x)_6Sn_5$ can thus be permanently assumed as the saturate concentration of Ni in $(Cu_{1-x}Ni_x)_6Sn_5$ of 32 at%. Assuming the diffusivity values of Ni through Cu_6Sn_5 reported in [138] in the order of 10^{-18} to 10^{-19} m^2/s with Ni concentrations of 0-30 at%, and using Van-Ostran Deway's solution to the diffusion equation, it would take more than 1600h of annealing at 200°C, and 800h of annealing at 260°C to reach 90% of the saturate concentration of Ni in 5µm of $(Cu_{1-x}Ni_x)_6Sn_5$. Once the saturate concentration is achieved, precipitation and growth of $(Ni_xCu_{1-x})_3Sn_4$ become thermodynamically favored, initiating at the interface between Ni and $(Cu_{1-x}Ni_x)_6Sn_5$. A mass spalling of $(Cu_{1-x}Ni_x)_6Sn_5$ was reported with decreasing concentrations of Cu, eventually resulting in the preferred formation of $(Ni_xCu_{1-x})_3Sn_4$ after annealing at 235°C [139]. This phenomenon was however only observed in presence of molten solder and with low Cu concentrations. In a similar isothermal aging study, this time in solid-state at 180°C, $(Cu_{1-x}Ni_x)_6Sn_5$ was identified as the dominant phase with a thin $(Ni_xCu_{1-x})_3Sn_4$ layer formed at the interface, even after 5000h of annealing [140]. High thermal stability is, therefore, theoretically expected with metastable SLID bonding.

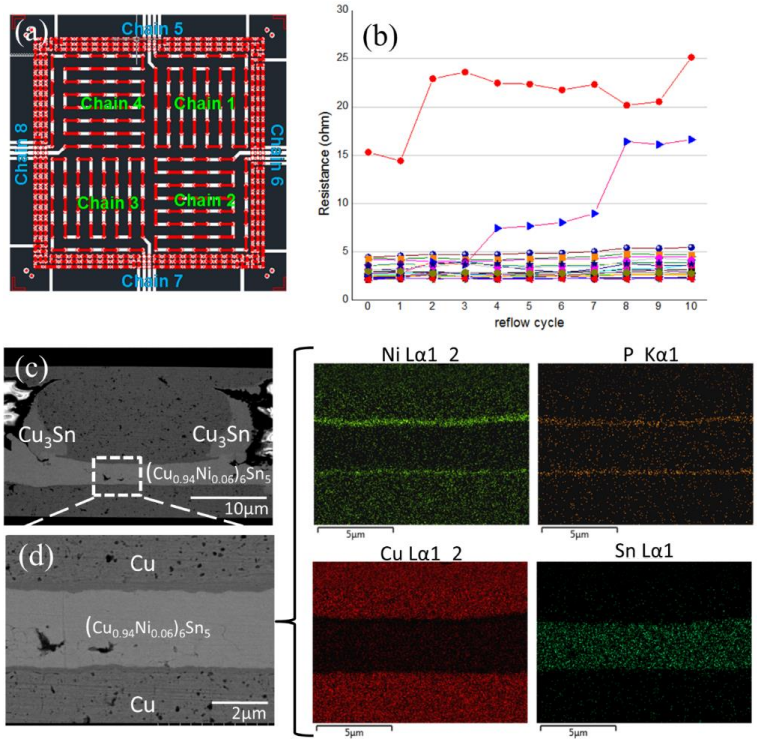


Figure 68. (a) Test vehicle design composed of eight daisy chains. (b) Daisy-chain electrical resistances monitored after each reflow cycle up to 10. (c) and (d) Micrographs and corresponding XEDS mapping showing the metastable interconnections after 10X reflow cycles.

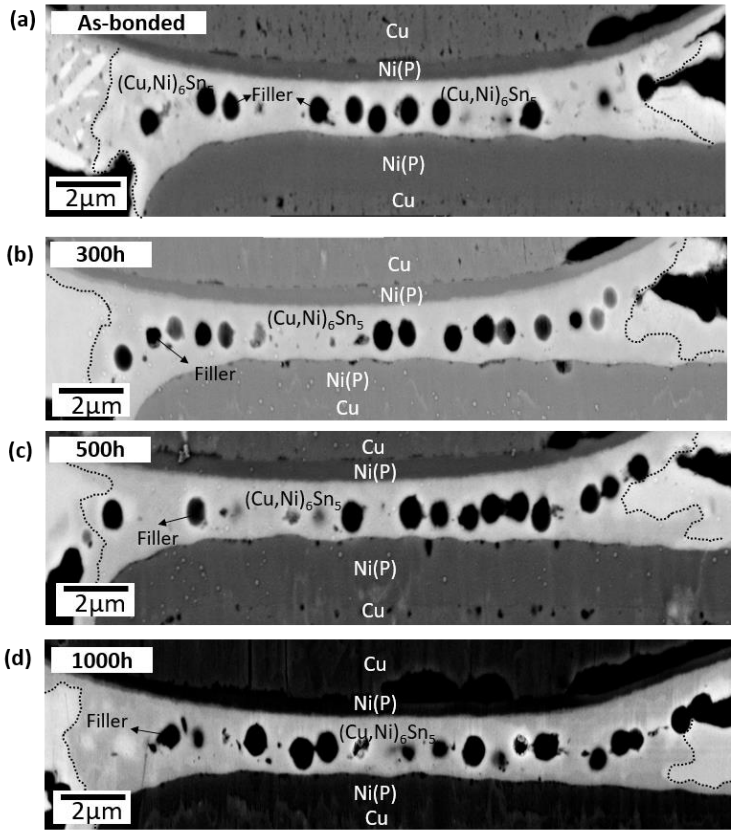


Figure 69. The semi-in situ SEM analysis with the assemblies of (a) as-bonded, and HTS for (b) 300h, (c) 500h, and (d) 1000h.

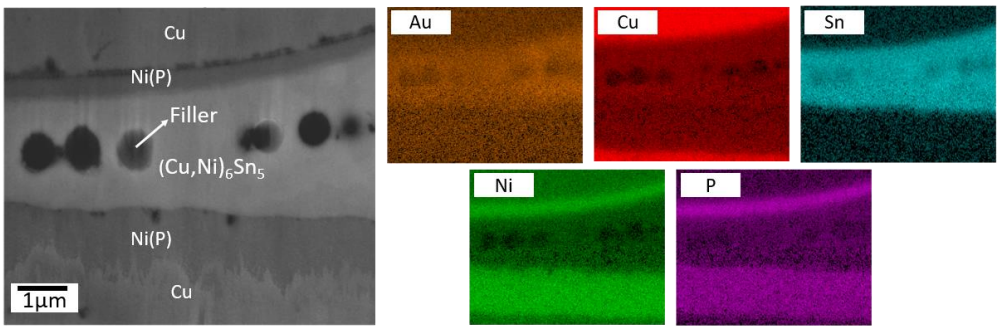


Figure 70. The zoom-in SEM image and corresponding XEDS mappings of the assemblies after 500h HTS.

7.3 Electromigration test

Electromigration testing was carried out at a current density of 10^5 A/cm^2 and an ambient temperature of 150°C. This current density is one to two orders of magnitude higher than the capability of traditional solders. An increase in as-bonded electrical resistance by 10% was used as failure criterion. No failures were observed after 500h of current stressing. The microstructural analysis of Fig. 71 indicates that the Ni(P) barrier and Cu bump were dissolved into Cu_6Sn_5 at the cathode while the Ni(P) barrier remained intact at the anode. Metal dissolution at the cathode interface prevailed in metastable SLID interconnections. With Cu and Ni from the cathode now involved in the interfacial reaction, Cu_3Sn and $(Cu_{0.44}Ni_{0.56})_6Sn_5$ were thus formed, with accompanying voids and micro-cracks distributed along the interface between Cu_3Sn and $(Cu_{0.44}Ni_{0.56})_6Sn_5$. Comparatively lower solubility of Ni in Cu_3Sn explains the absence of Ni in Cu_3Sn [141].

Compared to previous electromigration research, in which massive intermetallics were typically observed at the anode interface, Cu_3Sn was mainly found at the cathode interface in this study. This phenomenon can be explained by consideration of atomic flux under current stressing. The driving force from electron flow is roughly two orders of magnitude higher than that from the concentration gradient. The results were consequently dominated by electromigration. In solder interconnections, Cu atoms can easily be driven from the cathode to the anode through the solder which provides higher interstitial diffusivity of about 10^{-10} to 10^{-11} m^2/s at 150°C [129]. Intermetallics then form massively at the anode, caused by the excess of Cu atoms. In metastable SLID interconnections, Cu diffusion through the connecting layer was prevented by low diffusivity of Cu in Cu_6Sn_5, resulting in a higher Cu concentration near the cathode interface. Since solder was

completely consumed and transformed into $(Cu_{1-x}Ni_x)_6Sn_5$, accumulated Cu atoms could only react with $(Cu_{1-x}Ni_x)_6Sn_5$ to form Cu_3Sn.

These preliminary results indicate that 2µm-thick Ni barrier layers are not sufficient to survive such aggressive current stressing. The interconnection design was subsequently modified with 4µm-thick Ni barriers. The electromigration test was repeated on bumps with the new design. The SEM images of interconnections subjected to opposite electron current directions are shown in Fig. 72 after 1000h of current stressing. This time, distinct interfaces between Ni and $(Cu, Ni)_6Sn_5$ were observed, indicating that the dissolution challenge was solved with the modified stack-up.

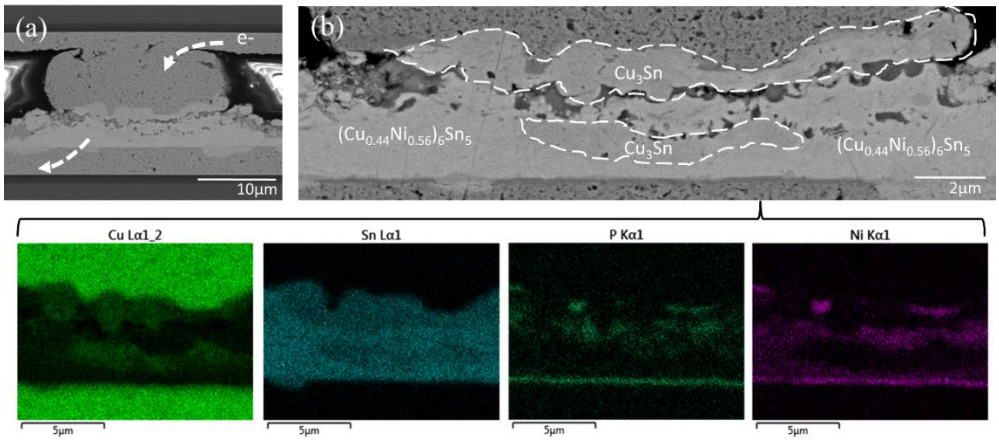


Figure 71. (a)(b) SEM images and XEDS mapping of metastable SLID interconnections with 2µm-thick Ni barriers after 500h of current stressing at 10^5 A/cm^2.

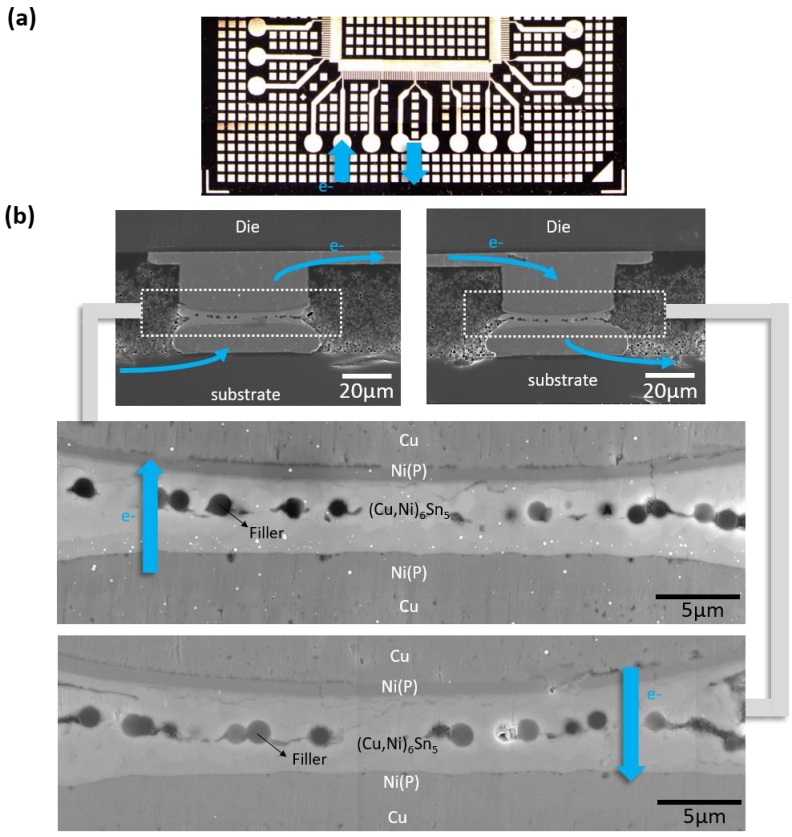
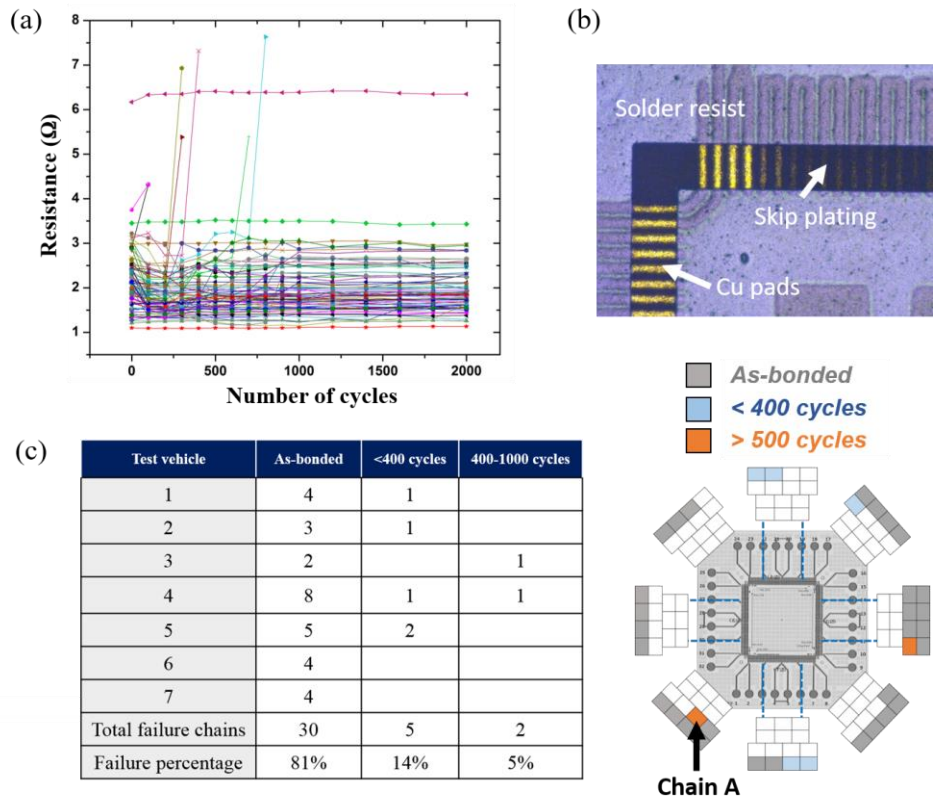


Figure 72. The (a) layout showing the direction of electron current, and (b) SEM images of metastable SLID interconnections with 4µm-thick Ni barriers after 1000h of current stressing at 10^5 A/cm^2.

7.4 Thermomechanical reliability test on 100µm-thick glass substrate

The daisy-chain test vehicle of TV2 was used for the first demonstration of the metastable SLID bonding technology on 100µm-thick, low-CTE glass substrates at 50µm pitch. The assembly process was designed based on the TC-NCP modeling described in Section 3.2, and the process optimization on thin glass substrate in Section 6.3.2. Metastable SLID interconnections with full transition to $(Cu_{1-x}Ni_x)_6Sn_5$ were successfully achieved, as shown in Fig. 66. A first screening of thermomechanical reliability was carried out by subjecting 7 assemblies to MSL-2 pre-conditionning, followed by thermal shock

test from -55℃ to 125℃, with a dwell time of 15min at each temperature extreme and 2 cycle/h in accordance to JEDEC-JESD22-A104C standards. Each assembled test vehicle comprises 16 daisy chains. The daisy chain resistances were monitored up to 2000 cycles, as shown in Fig. 73(a). The time to failure and failure distribution is reported in Fig. 73(c). Seven daisy chains, failed within 1000 cycles, were considered as the early failures. The remaining 75 daisy chains survived 2000 cycles. The failures before 400 cycles were attributed to process defects, including skip-plating of surface finish on substrate side and excessive bump non-coplanarities, as showed in Fig. 73(b). Later failures between 400 to 1000 cycles were caused by crack initiation and propagation at the interface between trapped silica fillers from the NCP material and intermetallics. Fig. 74 shows the SEM images of the open corner chain, highlighted as Chain A in the failure distribution of Fig. 73(c). With this open joint, the $(Ni, Cu)_3Sn_4$ was growing at the region beneath the cracks, while the $(Cu, Ni)_6Sn_5$ and Cu_3Sn were at the region above the cracks. This different composition distribution indicates an interfered interdiffusion cross the as-bonded joints, caused by the entrapped fillers. Since those failed joints were not composed of preferred intermetallics, the degraded reliability was expected. Filler entrapment has become a major reliability concern with reduction of solder volume and increase in filler content in advanced NCP materials that has yet to be fully addressed by the semiconductor industry. This issue is further aggravated with ultra-short as-plated bumps such as the metastable SLID interconnections. A novel bonding technologies such as ultrasonic-assisted bonding with NCF material are currently developing in industry.



(c)

Test vehicle	As-bonded	<400 cycles	400-1000 cycles
1	4	1	
2	3	1	
3	2		1
4	8	1	1
5	5	2	
6	4		
7	4		
Total failure chains	30	5	2
Failure percentage	81%	14%	5%

Figure 73. (a) Daisy-chain resistance monitoring through thermal shock test up to 2000 cycles; (b) photo of skip plating of ENIG on substrate; and (c) time to failure and failure distribution of tested daisy chains.

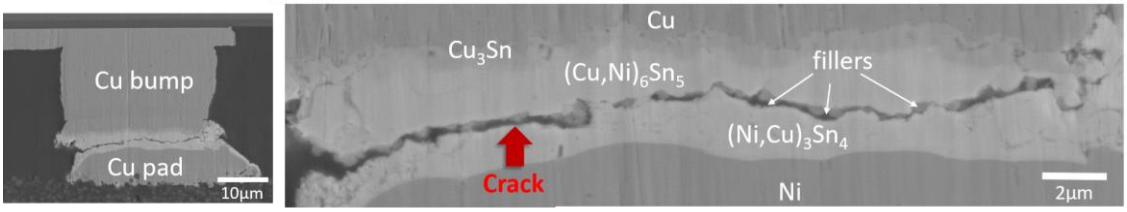


Figure 74. SEM images of failed interconnection, Chain A, after 2000 thermal-shock cycles.

7.5 First demonstration of 20µm-pitch off-chip interconnections

The TV3 at 20μm pitch was fabricated first on a 650μm-thick Si wafer, following the process decribed in Section 3.2.3. With the optimized lithography and plasma descum, the design metastable SLID bump structure was successfully fabricated with a bump diameter of 7μm. Fig. 75 shows the fabricated bumps, composed of a 1.2μm-thick Ni, 1.3μm-thick Cu, and 3.7μm-thick Sn, sat within the design tolerance. A thin Au layer was again used for adhesion of Ni and Sn. An ideal alignment was achieved with the APAMA Chip-to-Substrate Thermo-Compression Bonder from Kulicke & Soffa Corporation, which enabled a sub-micron coplanarites of the bond head and an accurate offset control of chip-to-substrate alignment. Fig. 76 shows the tilted view of X-ray image and the cross-section of bonded assemblies, in which the entire daisy chain was perfectly connected with 100% as-bonded yield. With the production flip-chip bonder, the designed bonding temperature of 260℃ was easily achieved with a peak bond head temperature of 290℃. A full transition to $(Cu, Ni)_6Sn_5$ was again achieved with a 1min dwell time at peak temperature, proved by the BEI images and XEDS mappings showed in Fig. 77. A superior pitch scalability was demonstrated with no risks of solder bridging granted by the extremely limited solder height of 3.7μm. The same substrate design of TV3 was then proceeded with a 300μm-thick 6-inch glass panel to demonstrate metastable SLID technology as the off-chip interconnection architecture. The Fig. 78(a) and (b, c) shows the fabricated glass substrate and the assemblies, respectively.

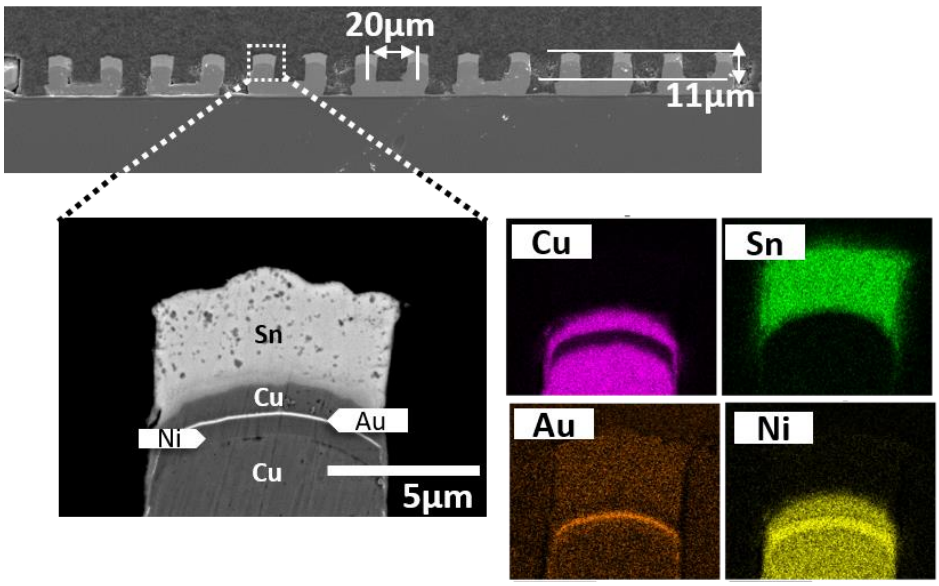


Figure 75. The fabricated metastable SLID bumps at 20µm pitch.

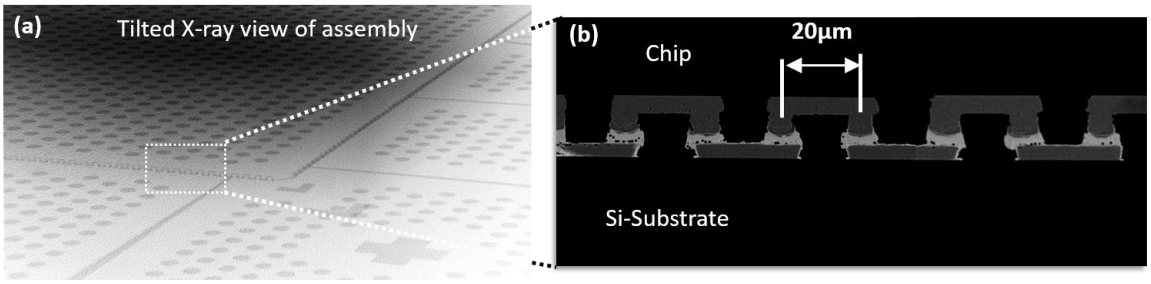


Figure 76. The (a) tilted x-ray view, and (b) BEI images of the assemblies.

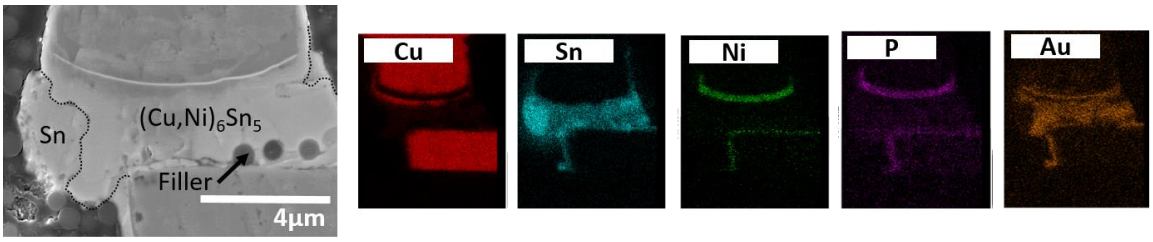


Figure 77. The SEM image and XEDS mappings with high magnification.

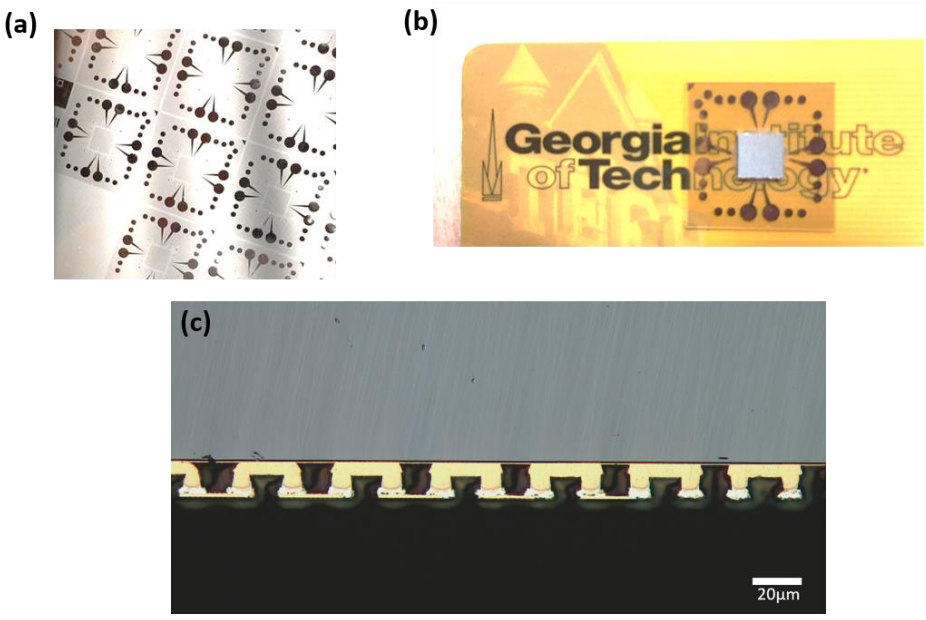


Figure 78. The (a) fabricated TV3 glass substrate, and the (b) top view and (c) cross-section of the assembled glass package.

7.6 Summary of metastable solid-liquid interdiffusion interconnection bonding

A new concept of metastable SLID bonding addressing the main challenges of standard SLID bonding was demonstrated for the first time in this thesis. An interdisciplinary design was first conducted with the aspects of material diffusion, phase transformation, thermomechanical reliability and high frequency electrical performance. By introducing Ni(P) barrier layers to control the interfacial reaction, all-intermetallic, void-free joints solely composed of $(Cu, Ni)_6Sn_5$ instead of Cu_3Sn were formed by 1min thermocompression bonding, with 20-30X improvements in assembly throughput. Metastable SLID interconnections exhibited superior shear strength of 88MPa due to their void-free single-phase composition. Outstanding thermal stability was verified through 10X standard reflow cycles with no observed daisy chain failures, as well as a 1000h high temperature storage at 150℃ without further phase transformation. The electromigration performance showed promising potential for this metastable SLID approach to handle ultra-high current densities of 10^5 A/cm^2, which is one order higher than the threshold current density of solder-capped Cu pillar. With the CTE-mismatched architecture, an outstanding thermomechanical reliability has been proved up to 2000 cycles with the die-to-glass-substrate configuration, beyond the state-of-arts of SLID bonding technology that are currently only adapted to 3D-ICs. Lastly, the metastable SLID bonding was successfully demonstrated at 20μm pitch with both 3D-IC and die-to-glass architecture. Metastable SLID was thus demonstrated as a compelling candidate of pitch scaling, and meanwhile satisfying the reliability requirements of not only 3D-ICs but off-chip interconnections in supercomputing 2.5D integration.

CHAPTER 8. SUMMARY AND CONCLUSIONS

This chapter summarizes the research work carried out in this thesis to improve pitch scalability, electrical and thermal performances as well as reliability of solder-based off-chip interconnections. The Cu pillar technology was first extended to 20μm pitch with less than 10μm solder height by fine control of interfacial reactions through design and optimization of assembly process and metallurgical system. The new metastable SLID concept was then introduced and demonstrated as a promising technology node beyond traditional solder approaches with superior power handling capability and thermal stability as well as improved manufacturability and reliability compared to existing SLID technologies. Recommendations for future work are also briefly discussed.

8.1 Research summary

The primary objective of this research was to extend the applicability of solder-based interconnections technology to pitches below 20μm to meet the integration density and performance needs of emerging high-performance systems. The interconnection system and assembly processes were designed from first principle to improve pitch scalability, electrical, thermal and reliability performances, as well as manufacturability beyond the capability of existing technologies. Three research tasks were defined to achieve these objectives: 1) Modeling, design and demonstration of TC-NCP on high-density ultra-thin glass substrates to provide guidelines for design of assembly processes with fine control of interfacial reactions; 2) Optimization of the interconnection system, focusing on surface finish metallurgies to control intermetallic formation for reliable, ultra-short Cu pillar interconnections; and 3) Modeling, design and demonstration of metastable

SLID bonding at 20µm pitch, addressing the limitations of solders in current-carrying capability and thermal stability and of standard SLID bonding in reliability and manufacturability.

8.1.1 Modeling, design and demonstration of TC-NCP for controlled reaction at fine pitch

In this research task, a strong modeling effort was undertaken to understand thermocompression bonding on a fundamental level, including interactions between tools, materials, package design and processes, so as to better control interfacial reactions and subsequent joints' microstructure.

A realistic electrical design of a multi-layered fully-integrated 100µm-thick glass substrate with BMVs and TPVs was considered. The thermal model of the fully-integrated package accounted for interactions with both the environment and the bonder and was used to determine the thermal gradient through the package in a standard TC-NCP process. A time-dependent thermal profile was applied on die side with varying tool head peak temperatures while the stage temperature was maintained at 70°C. With the same tool head peak temperature of 400°C, a significant temperature drop was observed in the solder, from 232℃ to 178℃, when increasing the number of metal routing layers. With the current trend towards ultra-thin high-density substrates, it becomes increasingly difficult to achieve metallurgical bonding within the thermal budget of existing production tools due to constraints on stage temperature with pre-applied underfill materials. A shift towards wafer-level pre-applied underfills such as non-conductive films (NCFs) might be necessary to address this challenges.

Estimation of the temperature distribution across the substrate in real time enabled identification of ideal thermal profiles to finely control interfacial reactions in TC-NCP. A couple-field process modeling was then developed, taking into account the actual temperature distribution extracted from the thermal model, the force profile and the NCP material. The corresponding solder collapse was subsequently predicted without hands-on trials and errors.

A parametric empirical study was finally carried out to validate modeling predictions, starting with the effect of substrate core thickness and metal loading. A study of the dynamic interaction between underfill curing and thermal profiles applied in TC-NCP concluded this work. Relying on excellent model-to-experiments correlation, the developed approach was confidently used to design TC-NCP processes for assembly on ultra-thin glass substrates with controlled intermtallic formation and solder collapse, and was successfully applied to several prototypes, including a 2.5D high-performance glass interposer. This work also initiated new focused research on TCB-induced warpage and system-level reliability in high-performance applications.

8.1.2 Optimization of interconnection system for reliable, ultra-short Cu pillar interconnections

Novel, ultra-thin, Ni-free electroless Pd (EP) and electroless Pd – autocatalytic Au (EPAG) surface finishes were introduced to improve pitch scalability of the Cu pillar technology, enabling for the first time reliable interconnections with reduced solder height of less than 10µm. EPAG and EP metallurgies in various compositions were evaluated and benchmarked against standard ENEPIG using first standard Cu pillar bumps with 15µm-

height solder cap and Ni diffusion barrier, then ultrashort Ni-free Cu pillars with 10µm-height solder cap. Such reduced solder height meets the design requirements for 20µm pitch, which is around 0.5× of the pitch size. It, therefore, can be used to assess pitch scalability of this technology. In this study, joints formed with standard ENEPIG showed significant embrittlement with formation of (Pd, Au)Sn_4 intermetallic and degraded reliability, regardless of the solder volume. However, EPAG and EP finishes performed differently with varying solder volumes.

With standard Cu pillar interconnections, the composition of EPAG and EP finishes was found to affect the as-bonded microstructure, but massive intermetallics were formed in all test cases after 500h high temperature storage. Further, a significant Cu consumption from the substrate wiring was observed in presence of a large amount of unreacted solder in thermal aging, as was theoretically predicted. As high-density 2.5D interposers typically involve ultra-thin traces, 1-5µm in thickness, excessive Cu consumption could have dramatic consequences and create opens in the wiring circuitry. Elimination of the Ni barrier layer between Cu pillar and solder cap was suggested to address this challenge and prevent Au embrittlement.

With a reduced solder height of 10µm, the microstructure and resulting reliability were dominated by the surface finish composition since the relative metal concentrations in solder were significantly increased. Detailed analysis of interfacial reactions through thermal aging indicated occurrence of embrittlement with ENEPIG, EPs and EPAGs in all but one composition. The Au embrittlement mechanisms were explained based on thermodynamics.

The EPAG-A composition exhibited a unique behavior with formation of a single intermetallic phase, $(Cu, Au, Pd)_6Sn_5$. The specific ratio of 50nm Au and 50nm Pd was, therefore, found critical in inhibiting gold embrittlement. Die shear and thermal shock tests confirmed the superiority of the EPAG-A composition. A shear strength of ~40MPa was achieved with EPAG-A, falling in the expected range for solder-based interconnections. The EPAG-A assemblies also survived over 500 cycles in a package configuration with high CTE mismatch, with a fatigue life nearing predictions from FEM modeling.

With this novel metallurgical system consisting of non-reflowed, Ni-free Cu pillar interconnections with solder caps less than 10µm in height, and a 50nmPd/50nmAu surface metallurgy applied on substrate pads, the Cu pillar technology can now satisfy the design rule of 20µm pitch. While such interconnection system can achieve the targeted I/O pitch, it cannot meet the increasing power handling, thermal stability and thermomechanical reliability requirements of future high-performance systems operating at higher temperatures. While the Ni-free Cu pillar is confirmed reliable for Cu pillar with 10µm solder, further pitch scaling and subsequent reduction in solder height is limited by the absence of barrier layer, in which solder would fully react and form all-intermetallic joints composed of dual Cu_6Sn_5 and Cu_3Sn compounds with unavoidable void formation degrading performance and reliability. The metastable SLID bonding technology was proposed to comprehensively address these remaining challenges with well-engineered intermetallic interconnections, designed from first principles to meet emerging pitch, performance and reliability requirements.

8.1.3 Metastable SLID bonding

A new concept of metastable SLID bonding was introduced to address the main challenges of standard SLID bonding: voiding, and bumping and assembly manufacturability. By introducing Ni(P) barrier layers to control the interfacial reaction, all-intermetallic, void-free joints solely composed of $(Cu, Ni)_6Sn_5$ instead of Cu_3Sn were formed. This specific intermetallic was selected based on the following benefits and design considerations:

- Lowest volume shrinkage of 3.9% through phase transformation within intermetallics commonly targeted in SLID systems
- High melting point of 638.4°C, giving high thermal stability
- Fast transition rate granted by liquid-phase reaction, as opposed to slow solid-state reactions required to reach stable phases
- High composition range of $(Cu, Ni)_6Sn_5$ brought by the substitution between Cu and Ni
- High mechanical modulus and low interstitutional diffusivities that enables high electromigration resistance
- Bump stack-up compatible with standard interconnection materials and processes for low-cost bumping

While traditional SLID bumps need an extremely accurate composition control, making for costly processes, the multi-layered metastable SLID bumps were designed to be highly manufacturable, with a tolerance to variations in composition 5X larger than standard plating processes capability. The interconnection system was also designed based on diffusion and kinetics modeling to achieve full transition to Cu_6Sn_5 within 1min at

260°C, which was successfully experimentally demonstrated, bringing a minimum 20X reduction in bonding time compared to standard SLID processes. A 2-step process using high-speed thermocompression bonding to initiate the reaction and a subsequent reflow step to reach the final composition was also proposed to further improve assembly throughput.

Metastable SLID interconnections exhibited superior shear strength of 88MPa owing to their void-free single-phase composition. Outstanding thermal stability was also verified through 10X standard reflow cycles and 200℃ high-temperature storage for 1000h, with no observed daisy-chain failures or further phase transformation. The electromigration performance showed promising potential for this metastable SLID approach to handle ultra-high current densities of 10^5 A/cm^2, beyond the capability of traditional solder-based interconnections. Thermomechanical reliability, targeted especially in package designs with substantial CTE mismatch, was demonstrated with 100µm-thick low-CTE glass substrates at 50µm pitch, passing over 1000 thermal-shock cycles. The metastable SLID was then scale to 20µm pitch, and demonstrated on both Si and glass substrates. Consequently, metastable SLID is believed to be a promising alternative to meet the performance and reliability needs of advanced 2.5D high-performance packaging.

8.1.4 Suggested future work

This research has studied many aspects of solder-based off-chip interconnections with an interdisciplinary approach to design with a focus on controlling interfacial reactions, and manufacturing considerations brought in by industry experts. From

technology perspective, three different interconnection systems were evaluated: standard and ultra-short Cu pillars as well as all-intermetallic joints. Metallurgical systems and assembly processes were designed and optimized through multi-physics modeling to enhance electrical, thermal and reliability performances while retaining the ease of processability and manufacturability of conventional solder-based approaches. A few future directions are suggested to complete this study and fully qualify the proposed technologies as a potential next interconnection node for high performance:

- With pitch scaling, interconnections shift from pre-reflowed solder bumps with rounded tip to non-reflowed bumps with extremely limited solder volume. In parallel, assembly moves from reflow to thermocompression bonding, typically with pre-applied materials. However, the use of NCP materials with high filler contents is very challenging with flat, ultra-short bumps, and typically result in filler entrapment in the connected layer. Wafer-level underfills, such as NCF, have gained momentum to address this challenge, but NCF materials are still in development and have limited flowability by design, which brings voiding concerns in die-to-substrate assemblies. As an alternative, ultrasonic bonding is now being explored to not only potentially reduce filler entrapment, but also further improve the transition rate of metastable SLID bonding. With added ultrasonic energy, the 1min bonding time could theoretically be reduced to less than 10s.
- While initial themomechanical reliability of metastable SLID bonding has been proven through modeling and experiments, this reliability

assessment was performed on non-functional wafers. The shift from soft solders to more rigid intermetallic joints is known to yield potential cracking of BEOL ultra-low-K dielectric layers, a major reliability concern. Preliminary FEM modeling was carried out and showed promising results, in which compressive stresses introduced by pre-applied underfills bring down the energy release rate (G-integral) at the crack tip, effectively preventing crack propagation in the ultra-low-K layer. A new, functional test vehicle is however required to validate modeling predictions. Such test vehicle is currently being fabricated by Global Foundries.

- Nickel was selected as diffusion barrier to block the Cu flux from bumps and pads for the first demonstration of the metastable SLID bonding concept. To address concerns of degraded electrical performance in presence of Ni, AC and DC modeling were performed to optimize the bump design to match the performance of standard Cu pillars. However, new materials should be explored to realize the Cu diffusion barriers, especially with sub-micron thicknesses. Ni has been the packaging material of choice for diffusion barrier for decades, so finding a suitable replacement candidate that would meet industry's acceptance is very challenging and would necessitate leveraging existing infrastructure and processes. An ideal candidate material should survive temperatures of 260°C with direct contact with molten solder, have a high electromigration resistance and be compatible with standard bumping

processes at low cost. Although recent studies have shown the potential of some CVD-grown layers, such as TiN or Ti/TiN in efficiently blocking Cu diffusion, their application was limited to transistor level. Focused research in Cu diffusion barrier materials is a strategic need to scale solder-based interconnection technologies.

This research is a critical building block to enable future 2.5D high-performance packages with a terabit per second die-to-die bandwidth. The interconnection and assembly technologies developed in this work will soon be applied at GT-PRC to build a fully-integrated, ultra-thin 2.5D glass interposer package at 20μm off-chip interconnection pitch.

8.2 Conclusions

This thesis work was conducted to extend pitch scalability, thermal stability and power handling capability of solder-based interconnections to meet the needs of emerging high-performance computing applications. The fundamental focus was on controlling interfacial reactions through multi-physics design of interconnection systems and assembly processes, which becomes more and more critical as the solder height scales down with pitch. The Cu pillar technology was first successfully scaled down to sub-10μm solder height, enabled by the optimization of the metallurgical system with the new EPAG surface finish and of TC-NCP processes for finely controlled assembly. The metastable SLID bonding was then designed and demonstrated at 20μm pitch with superior thermal stability at 200℃ and power handling at 10^5 A/cm^2. This thesis has confirmed the capability of solder-based interconnections to satisfy the coming needs of electronic systems using material science theories to design metallurgical systems and assembly processes with fine control of phase transformation, while keeping processability manufacturing-friendly.

Some scientific and technical contributions were been made in this thesis. In research task 1, this thesis estabilished a methodology of coupling the FEM modelings with experimental inputs. The modeling parameters were fitted according to the measured results, and the boundary conditions of multiphysics process modeling were set based on the understandings of material behaviors. This process modeling indeed shows the possibility of capturing the transient behavior of complicated manufacturing process through FEM. In research task 2, this thesis successfully aligned up the fundamental microstructure analysis with industry-centric reliability requirements, and provided theoretic explanation and proposed solution of observed phenomenon. In research task 3, the interdisciplinary design guidelines with the aspects of material science, mechanical and electrical engineering were first provided to establish the metallurgical system. The consideration of manufacturability was then taken into account, bridging the capability of electronic manufacturing with academia. Lastly, the experimental evaluations were defined corresponding to the design and research objectives.

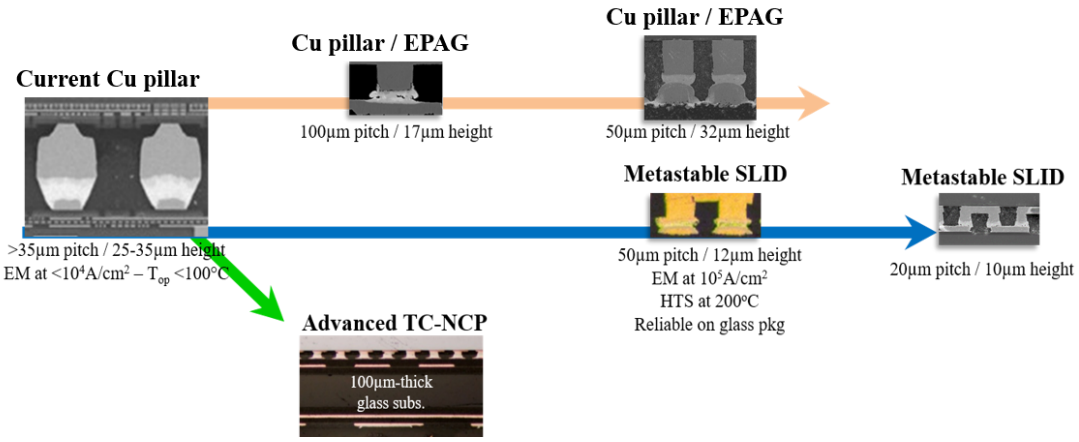


Figure 79. Summary of pitch and performance scaling of solder-based interconnections through multi-physics design of interconnection systems and assembly processes.

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